

International **IOR** Rectifier

80RIA SERIES

PHASE CONTROL THYRISTORS

Stud Version

Features

- Hermetic glass-metal seal
- International standard case TO-209AC (TO-94)

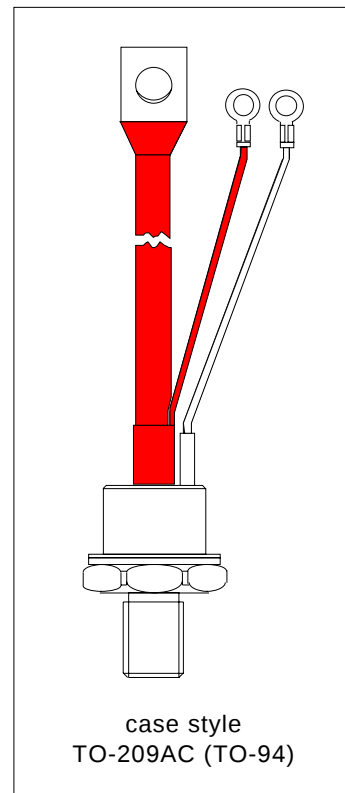
80A

Typical Applications

- DC motor controls
- Controlled DC power supplies
- AC controllers

Major Ratings and Characteristics

Parameters	80RIA	Unit
$I_{T(AV)}$	80	A
@ T_C	85	°C
$I_{T(RMS)}$	125	A
I_{TSM} @ 50Hz	1900	A
@ 60Hz	1990	A
I^2t @ 50Hz	18	KA ² s
@ 60Hz	16	KA ² s
V_{DRM}/V_{RRM}	400 to 1200	V
t_q typical	110	μs
T_J	- 40 to 125	°C



ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	Voltage Code	V_{DRM}/V_{RRM} , max. repetitive peak and off-state voltage V	V_{RSM} , maximum non-repetitive peak voltage V	I_{DRM}/I_{RRM} max. @ $T_J = 125^\circ\text{C}$ mA
80RIA	40	400	500	15
	80	800	900	
	120	1200	1300	

On-state Conduction

Parameter		80RIA	Units	Conditions			
I _{T(AV)}	Max. average on-state current @ Case temperature	80	A	180° conduction, half sine wave			
		85	°C				
I _{T(RMS)}	Max. RMS on-state current	125	A	DC @ 75°C case temperature			
I _{TSM}	Max. peak, one-cycle non-repetitive surge current	1900	A	t = 10ms	No voltage	Sinusoidal half wave, Initial T _J = T _J max.	
		t = 8.3ms		reapplied			
		1600		t = 10ms	100% V _{RRM}		
		1675		t = 8.3ms	reapplied		
I ² t	Maximum I ² t for fusing	18	KA ² s	t = 10ms	No voltage		
		16		t = 8.3ms	reapplied		
		12.7		t = 10ms	100% V _{RRM}		
		11.7		t = 8.3ms	reapplied		
I ² √t	Maximum I ² √t for fusing	180.5	KA ² √s	t = 0.1 to 10ms, no voltage reapplied			
V _{T(TO)1}	Low level value of threshold voltage	0.99	V	(16.7% × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J max.			
V _{T(TO)2}	High level value of threshold voltage	1.13		(I > π × I _{T(AV)}), T _J = T _J max.			
r _{t1}	Low level value of on-state slope resistance	2.29	mΩ	(16.7% × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J max.			
r _{t2}	High level value of on-state slope resistance	1.84		(I > π × I _{T(AV)}), T _J = T _J max.			
V _{TM}	Max. on-state voltage	1.60	V	I _{pk} = 250A, T _J = 25°C t _p = 10ms sine pulse			
I _H	Maximum holding current	200	mA	T _J = 25°C, anode supply 12V resistive load			
I _L	Typical latching current	400					

Switching

Parameter	80RIA	Units	Conditions
di/dt Max. non-repetitive rate of rise of turned-on current	300	A/ μ s	$T_J = 125^\circ\text{C}$, $V_d = \text{rated } V_{\text{DRM}}$, $I_{\text{TM}} = 2 \times di/dt$ snubber $0.2\mu\text{F}$, 15Ω , Gate pulse: 20V , 65Ω , $t_p = 6\mu\text{s}$, $t_r = 0.5\mu\text{s}$ Per JEDEC Standard RS-397, 5.2.2.6.
t_d Typical delay time	1	μs	Gate pulse: 10V , 15Ω source, $t_p = 6\mu\text{s}$, $t_r = 0.1\mu\text{s}$, $V_d = \text{rated } V_{\text{DRM}}$, $I_{\text{TM}} = 50\text{Adc}$, $T_J = 25^\circ\text{C}$.
t_q Typical turn-off time	110		$I_{\text{TM}} = 50\text{A}$, $T_J = T_J \text{ max}$, $di/dt = -5\text{A}/\mu\text{s min.}$, $V_R = 50\text{V}$, $dv/dt = 20\text{V}/\mu\text{s}$, Gate bias: 0V 25Ω , $t_p = 500\mu\text{s}$

Blocking

Parameter	80RIA	Units	Conditions
dv/dt Maximum critical rate of rise of off-state voltage	500	V/ μ s	$T_J = 125^\circ\text{C}$ exponential to 67% rated V_{DRM}
I_{RRM} I_{DRM} Max. peak reverse and off-state leakage current	15	mA	$T_J = 125^\circ\text{C}$ rated $V_{\text{DRM}}/V_{\text{RRM}}$ applied

Triggering

Parameter	80RIA	Units	Conditions
P_{GM} Maximum peak gate power	12	W	$T_J = T_J \text{ max}$, $t_p \leq 5\text{ms}$
$P_{\text{G(AV)}}$ Maximum average gate power	3		$T_J = T_J \text{ max}$, $f = 50\text{Hz}$, $d\% = 50$
I_{GM} Max. peak positive gate current	3	A	$T_J = T_J \text{ max}$, $t_p \leq 5\text{ms}$
$+V_{\text{GM}}$ Maximum peak positive gate voltage	20	V	$T_J = T_J \text{ max}$, $t_p \leq 5\text{ms}$
$-V_{\text{GM}}$ Maximum peak negative gate voltage	10		
I_{GT} Max. DC gate current required to trigger	270	mA	$T_J = -40^\circ\text{C}$
	120		$T_J = 25^\circ\text{C}$
	60		$T_J = 125^\circ\text{C}$
V_{GT} Max. DC gate voltage required to trigger	3.5	V	$T_J = -40^\circ\text{C}$
	2.5		$T_J = 25^\circ\text{C}$
	1.5		$T_J = 125^\circ\text{C}$
I_{GD} DC gate current not to trigger	6	mA	$T_J = T_J \text{ max}$ Max. gate current/ voltage not to trigger is the max. value which will not trigger any unit with rated V_{DRM} anode-to-cathode applied
V_{GD} DC gate voltage not to trigger	0.25	V	

80RIA Series

Bulletin I25201 rev. B 03/03

International
IRF Rectifier

Thermal and Mechanical Specification

Parameter	80RIA	Units	Conditions
T_J Max. operating temperature range	-40 to 125	°C	
T_{stg} Max. storage temperature range	-40 to 150		
R_{thJC} Max. thermal resistance, junction to case	0.30	K/W	DC operation
R_{thCS} Max. thermal resistance, case to heatsink	0.1		Mounting surface, smooth, flat and greased
T Mounting torque, $\pm 10\%$	15.5 (137)	Nm	Non lubricated threads
	14 (120)	(lbf-in)	Lubricated threads
wt Approximate weight	130	g	
Case style	TO-209AC(TO-94)		See Outline Table

ΔR_{thJ-C} Conduction

(The following table shows the increment of thermal resistance R_{thJ-C} when devices operate at different conduction angles than DC)

Conduction angle	Sinusoidal conduction	Rectangular conduction	Units	Conditions
180°	0.042	0.030	K/W	$T_J = T_J \text{ max.}$
120°	0.050	0.052		
90°	0.064	0.070		
60°	0.095	0.100		
30°	0.164	0.165		

Ordering Information Table

Device Code

- 1** - $I_{TAV} \times 10A$
- 2** - 0 = Eyelet terminals (Gate and Auxiliary Cathode Leads)
1 = Fast - on terminals (Gate and Auxiliary Cathode Leads)
- 3** - RIA = Essential part number
- 4** - Voltage code: Code $\times 10 = V_{RRM}$ (See Voltage Rating Table)
- 5** - None = Stud base 1/2"-20UNF- 2A threads

NOTE: For Metric Device M12 x 1.75 E6 Contact factory

Outline Table

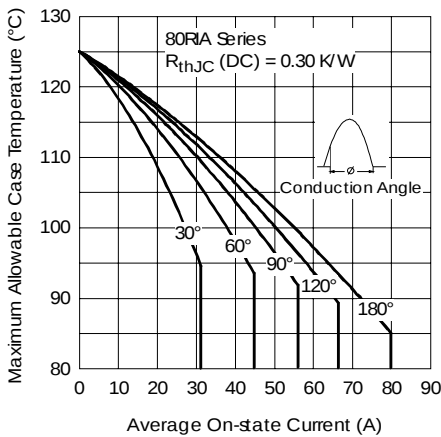
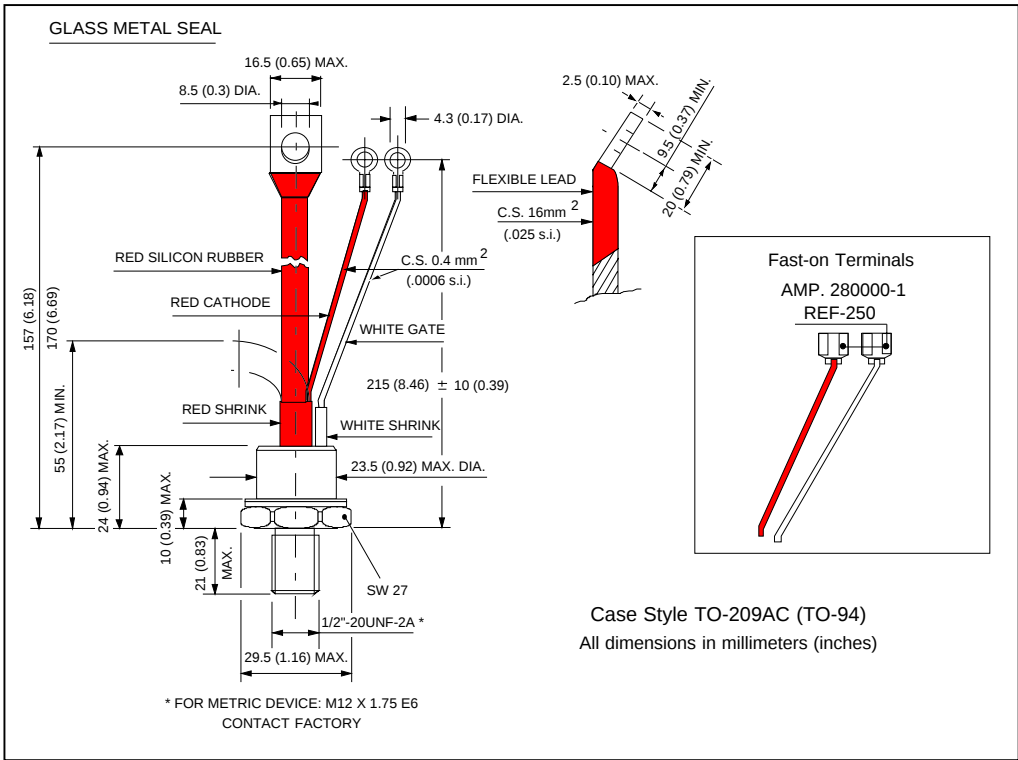


Fig. 1 - Current Ratings Characteristics

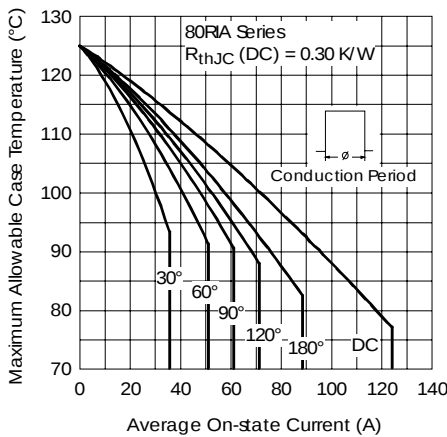


Fig. 2 - Current Ratings Characteristics

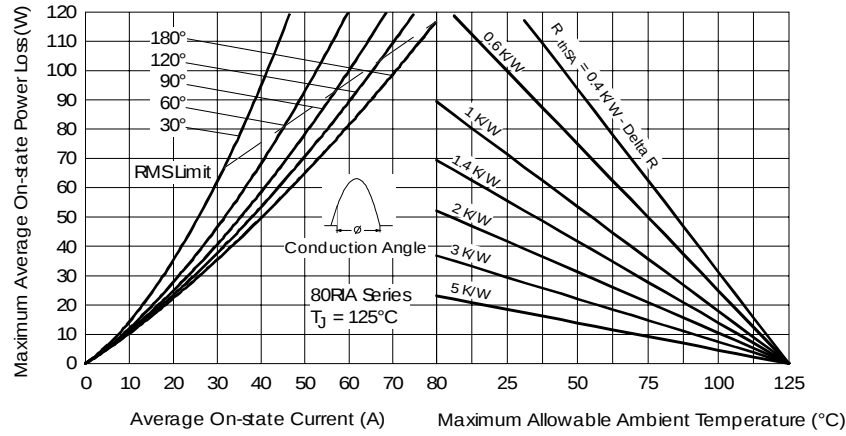


Fig. 3 - On-state Power Loss Characteristics

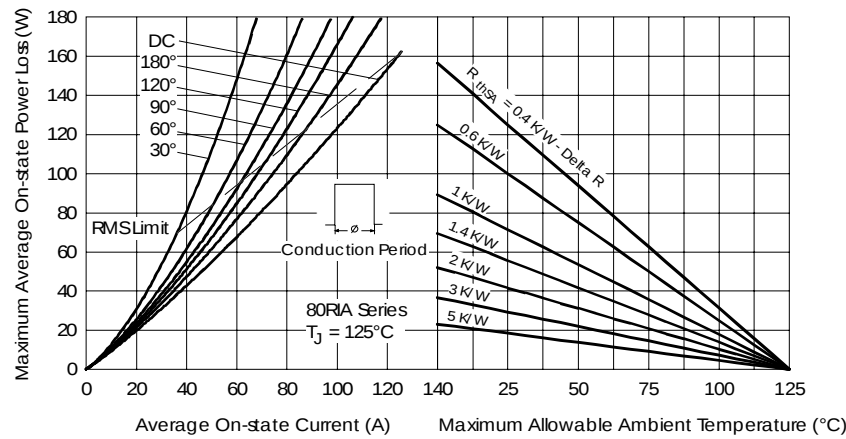


Fig. 4 - On-state Power Loss Characteristics

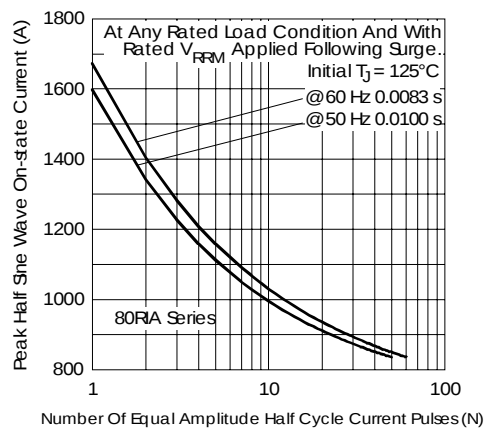


Fig. 5 - Maximum Non-Repetitive Surge Current

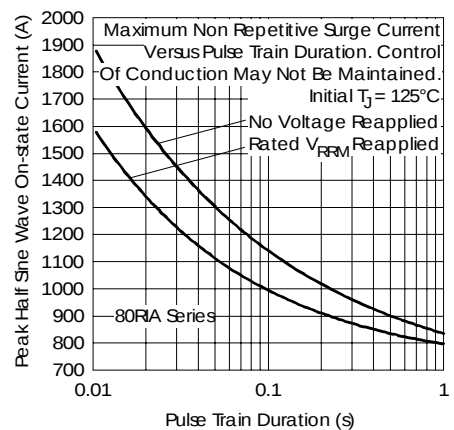


Fig. 6 - Maximum Non-Repetitive Surge Current

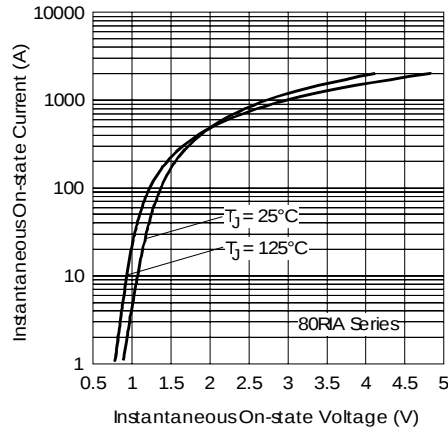


Fig. 7 - On-state Voltage Drop Characteristics

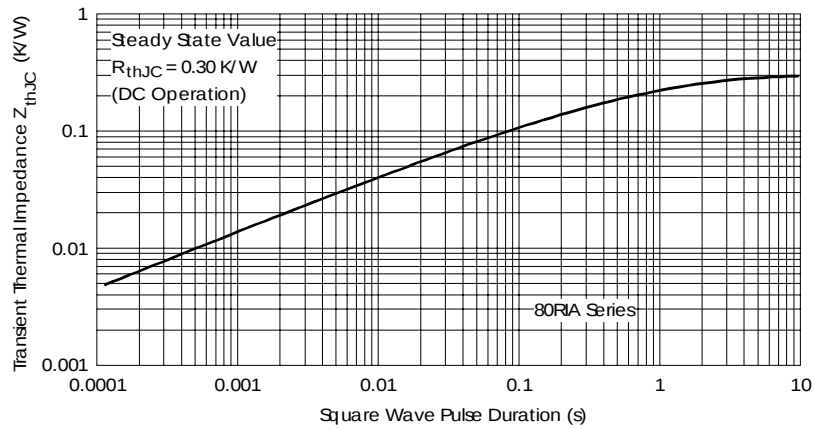


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

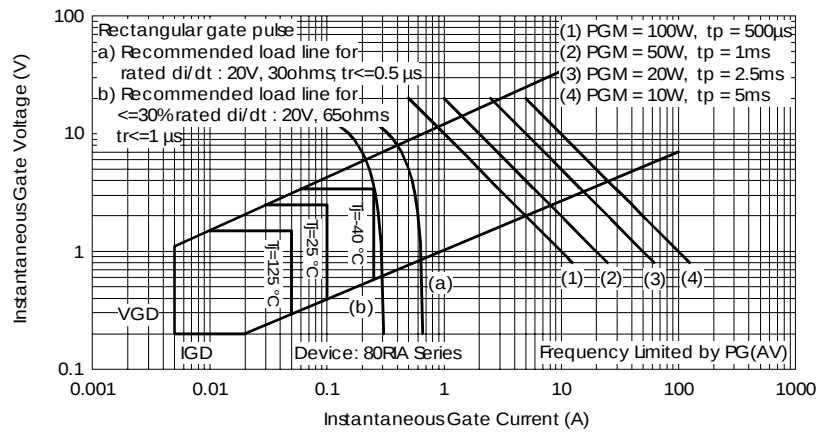


Fig. 9 - Gate Characteristics

80RIA Series

Bulletin I25201 rev. B 03/03

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Data and specifications subject to change without notice.
This product has been designed and qualified for Industrial Level.
Qualification Standards can be found on IR's Web site.

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