

TENTATIVE

CM100DC-24NFM

Pre.	S.Kawabata,H.Takemoto,M.Hiyoshi	Rev	
Apr.	Y.Nagashima 1-Dec-'06		

HIGH POWER SWITCHING USE

Notice: This is not a final specification. Some parametric limits are subject to change.

CM100DC-24NFM	
I_C	100A
V_{CES}	1200V
Insulated Type	
2-elements in a pack	

Caution: No short circuit capability is designed.

APPLICATION

High frequency switching use & Resonant inverter power supply, etc

ABSOLUTE MAXIMUM RATINGS ($T_j=25^\circ\text{C}$, unless otherwise specified)

Symbol	Item	Conditions	Ratings	Units
V_{CES}	Collector-emitter voltage	G-E Short	1200	V
V_{GES}	Gate-emitter voltage	C-E Short	± 20	V
I_C	Collector current	Operation	100	A
I_{CM}		Pulse ^{*4}	200	
I_E ^{*3}	Emitter current	Operation	100	A
I_{EM} ^{*3}		Pulse ^{*4}	200	
P_C ^{*5}	Maximum collector dissipation	$T_C=25^\circ\text{C}$ ^{*1}	670	W
T_j	Junction temperature		- 40 ~ +150	$^\circ\text{C}$
T_{stg}	Storage temperature		- 40 ~ +125	$^\circ\text{C}$
V_{iso}	Isolation voltage	Main terminal to base plate, AC 1 min.	2500	V
-	Torque strength	Main terminal M6	3.5 ~ 4.5	N·m
-	Torque strength	Mounting holes M6	3.5 ~ 4.5	N·m
-	Weight	Typical value	375	g

ELECTRICAL CHARACTERISTICS ($T_j=25^{\circ}\text{C}$, unless otherwise specified)

Symbol	Item	Conditions	Min.	Typ.	Max.	Units	
I_{CES}	Collector cutoff current	$V_{CE}=V_{CES}$, $V_{GE}=0\text{V}$	-	-	1	mA	
$V_{GE(th)}$	Gate-emitter threshold voltage	$I_C=10\text{mA}$, $V_{CE}=10\text{V}$	4.5	6.0	7.5	V	
I_{GES}	Gate leakage current	$\pm V_{GE}=V_{GES}$, $V_{CE}=0\text{V}$	-	-	0.5	μA	
$V_{CE(sat)}$	Collector to emitter saturation voltage	$I_C=100\text{A}$ ^{*6}	-	$T_j=25^{\circ}\text{C}$	3.0	4.5	V
		$V_{GE}=15\text{V}$		$T_j=125^{\circ}\text{C}$	3.0	-	
C_{ies}	Input capacitance	$V_{GE}=0\text{V}$, $V_{CE}=10\text{V}$ ^{*6}	-	-	16	nF	
C_{oes}	Output capacitance		-	-	1.3		
C_{res}	Reverse transfer capacitance		-	-	0.3		
Q_G	Total gate charge	$V_{CC}=600\text{V}$, $I_C=100\text{A}$, $V_{GE}=15\text{V}$	-	450	-	nC	
$t_{d(on)}$	Turn-on delay time	$V_{CC}=600\text{V}$, $I_C=100\text{A}$	-	-	100	ns	
t_r	Turn-on rise time	$V_{GE1}=V_{GE2}=15\text{V}$, $R_G=3.1\Omega$	-	-	50		
$t_{d(off)}$	Turn-off delay time	Inductive load	-	-	250		
t_f	Turn-off fall time	switching operation	-	60	200		
t_{rr} ^{*3}	Reverse recovery time	$I_E=100\text{A}$	-	70	120		
Q_{rr} ^{*3}	Reverse recovery charge		-	6	-	μC	
V_{EC} ^{*3}	Emitter-collector voltage	$I_E=100\text{A}$, $V_{GE}=0\text{V}$	-	2.0	3.0	V	
$R_{th(j-c)Q}$	Thermal resistance	IGBT part (1/2 module) ^{*1}	-	-	0.186	$^{\circ}\text{C/W}$	
$R_{th(j-c)R}$		FWDi part (1/2 module) ^{*1}	-	-	0.28		
$R_{th(c-f)}$	Contact thermal resistance	Case to fin, Thermal grease applied (1/2module) ^{*1 *2}	-	0.02	-		
R_G	External gate resistance		3.1	-	31	Ω	

*1: T_C , T_f measured point is just under the chips.

*2: Typical value is measured by using Shin-Etsu Chemical Co.,Ltd "G-747".

*3: I_E , I_{EM} , V_{EC} , t_{rr} & Q_{rr} represent characteristics of the anti-parallel, emitter to collector free-wheel diode (FWDi).

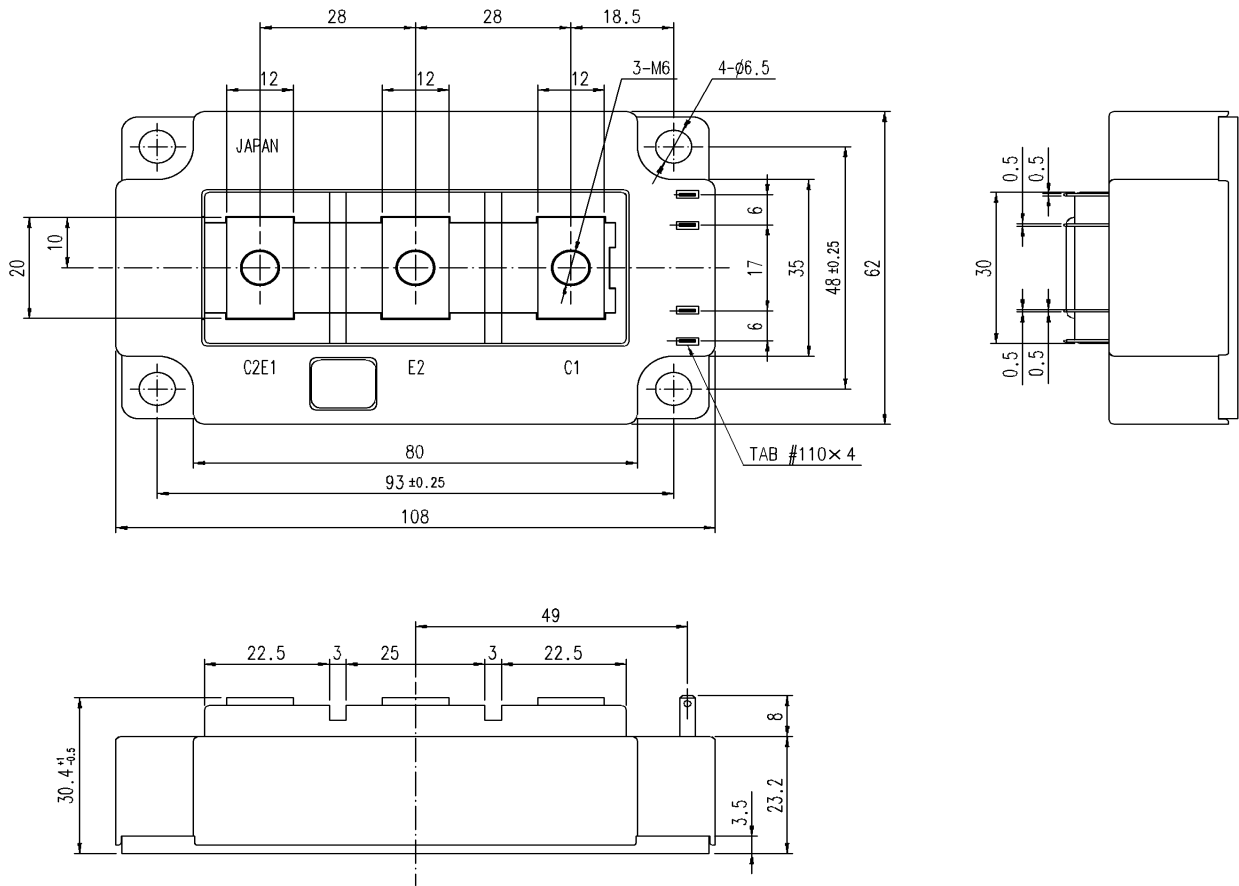
*4: Pulse width and repetition rate should be such that the device junction temperature (T_j) dose not exceed T_{jmax} rating.

*5: Junction temperature (T_j) should not increase beyond 150°C .

*6: Pulse width and repetition rate should be such as to cause negligible temperature rise.

OUTLINE DRAWING

Dimensions in mm



CIRCUIT DIAGRAM

