

### HIGH AND LOW SIDE DRIVER

#### Features

- Floating channel designed for bootstrap operation  
Fully operational to +600V  
Tolerant to negative transient voltage  
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 3.3V, 5V, and 15V logic input compatible
- Matched propagation delay for both channels
- Outputs in phase with inputs (IR2101) or out of phase with inputs (IR2102)

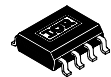
#### Description

The IR2101(S)/IR2102(S) are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

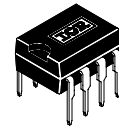
#### Product Summary

|                            |                 |
|----------------------------|-----------------|
| $V_{\text{OFFSET}}$        | 600V max.       |
| $I_{\text{O+/-}}$          | 130 mA / 270 mA |
| $V_{\text{OUT}}$           | 10 - 20V        |
| $t_{\text{on/off (typ.)}}$ | 160 & 150 ns    |
| Delay Matching             | 50 ns           |

#### Packages

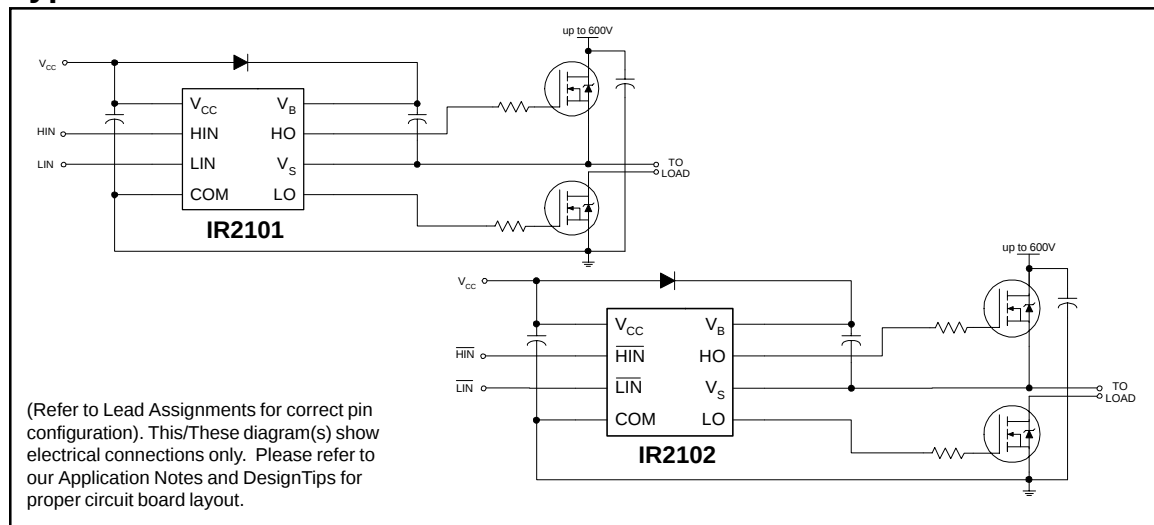


8 Lead SOIC



8 Lead PDIP

#### Typical Connection



# IR2101/IR2102 (S)

International  
**IR** Rectifier

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

| Symbol     | Definition                                               | Min.          | Max.           | Units              |
|------------|----------------------------------------------------------|---------------|----------------|--------------------|
| $V_B$      | High side floating supply voltage                        | -0.3          | 625            | V                  |
| $V_S$      | High side floating supply offset voltage                 | $V_B - 25$    | $V_B + 0.3$    |                    |
| $V_{HO}$   | High side floating output voltage                        | $V_S - 0.3$   | $V_B + 0.3$    |                    |
| $V_{CC}$   | Low side and logic fixed supply voltage                  | -0.3          | 25             |                    |
| $V_{LO}$   | Low side output voltage                                  | -0.3          | $V_{CC} + 0.3$ |                    |
| $V_{IN}$   | Logic input voltage (HIN & LIN)                          | -0.3          | $V_{CC} + 0.3$ |                    |
| $dV_S/dt$  | Allowable offset supply voltage transient                | —             | 50             | V/ns               |
| $P_D$      | Package power dissipation @ $T_A \leq +25^\circ\text{C}$ | (8 lead PDIP) | 1.0            | W                  |
|            |                                                          | (8 lead SOIC) | 0.625          |                    |
| $R_{thJA}$ | Thermal resistance, junction to ambient                  | (8 lead PDIP) | 125            | $^\circ\text{C/W}$ |
|            |                                                          | (8 lead SOIC) | 200            |                    |
| $T_J$      | Junction temperature                                     | —             | 150            | $^\circ\text{C}$   |
| $T_S$      | Storage temperature                                      | -55           | 150            |                    |
| $T_L$      | Lead temperature (soldering, 10 seconds)                 | —             | 300            |                    |

## Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The  $V_S$  offset rating is tested with all supplies biased at 15V differential.

| Symbol   | Definition                                                                                                | Min.       | Max.       | Units            |
|----------|-----------------------------------------------------------------------------------------------------------|------------|------------|------------------|
| $V_B$    | High side floating supply absolute voltage                                                                | $V_S + 10$ | $V_S + 20$ | V                |
| $V_S$    | High side floating supply offset voltage                                                                  | Note 1     | 600        |                  |
| $V_{HO}$ | High side floating output voltage                                                                         | $V_S$      | $V_B$      |                  |
| $V_{CC}$ | Low side and logic fixed supply voltage                                                                   | 10         | 20         |                  |
| $V_{LO}$ | Low side output voltage                                                                                   | 0          | $V_{CC}$   |                  |
| $V_{IN}$ | Logic input voltage (HIN & LIN) (IR2101) & ( $\overline{\text{HIN}}$ & $\overline{\text{LIN}}$ ) (IR2102) | 0          | $V_{CC}$   |                  |
| $T_A$    | Ambient temperature                                                                                       | -40        | 125        | $^\circ\text{C}$ |

**Note 1:** Logic operational for  $V_S$  of -5 to +600V. Logic state held for  $V_S$  of -5V to  $-V_{BS}$ . (Please refer to the Design Tip DT97-3 for more details).

## Dynamic Electrical Characteristics

V<sub>BIAS</sub> (V<sub>CC</sub>, V<sub>BS</sub>) = 15V, C<sub>L</sub> = 1000 pF and T<sub>A</sub> = 25°C unless otherwise specified.

| Symbol           | Definition                          | Min. | Typ. | Max. | Units | Test Conditions       |
|------------------|-------------------------------------|------|------|------|-------|-----------------------|
| t <sub>on</sub>  | Turn-on propagation delay           | —    | 160  | 220  | ns    | V <sub>S</sub> = 0V   |
| t <sub>off</sub> | Turn-off propagation delay          | —    | 150  | 220  |       | V <sub>S</sub> = 600V |
| t <sub>r</sub>   | Turn-on rise time                   | —    | 100  | 170  |       |                       |
| t <sub>f</sub>   | Turn-off fall time                  | —    | 50   | 90   |       |                       |
| MT               | Delay matching, HS & LS turn-on/off | —    | —    | 50   |       |                       |

## Static Electrical Characteristics

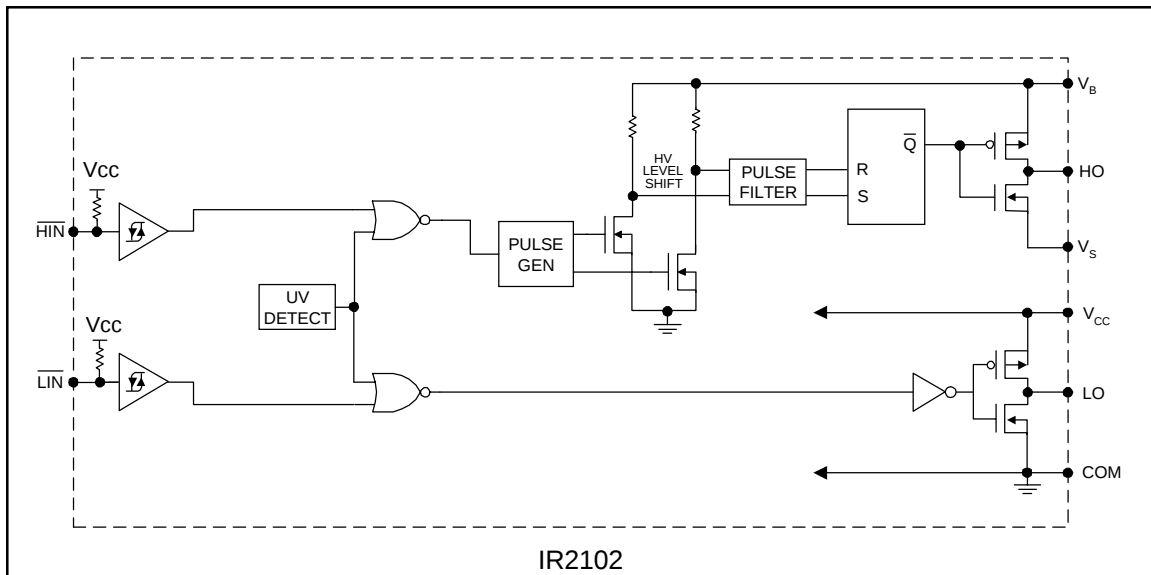
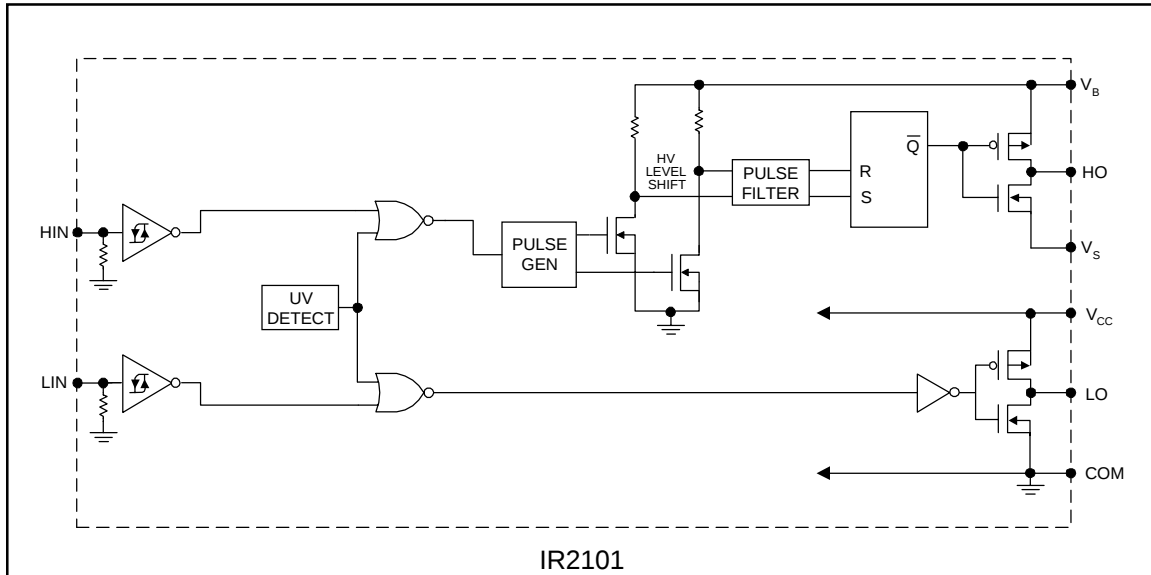
V<sub>BIAS</sub> (V<sub>CC</sub>, V<sub>BS</sub>) = 15V and T<sub>A</sub> = 25°C unless otherwise specified. The V<sub>IN</sub>, V<sub>TH</sub> and I<sub>IN</sub> parameters are referenced to COM. The V<sub>O</sub> and I<sub>O</sub> parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

| Symbol             | Definition                                                           | Min. | Typ. | Max. | Units | Test Conditions                                                   |
|--------------------|----------------------------------------------------------------------|------|------|------|-------|-------------------------------------------------------------------|
| V <sub>IH</sub>    | Logic "1" input voltage (IR2101)<br>Logic "0" input voltage (IR2102) | 3    | —    | —    | V     | V <sub>CC</sub> = 10V to 20V                                      |
| V <sub>IL</sub>    | Logic "0" input voltage (IR2101)<br>Logic "1" input voltage (IR2102) | —    | —    | 0.8  |       | V <sub>CC</sub> = 10V to 20V                                      |
| V <sub>OH</sub>    | High level output voltage, V <sub>BIAS</sub> - V <sub>O</sub>        | —    | —    | 100  | mV    | I <sub>O</sub> = 0A                                               |
| V <sub>OL</sub>    | Low level output voltage, V <sub>O</sub>                             | —    | —    | 100  |       | I <sub>O</sub> = 0A                                               |
| I <sub>LK</sub>    | Offset supply leakage current                                        | —    | —    | 50   | μA    | V <sub>B</sub> = V <sub>S</sub> = 600V                            |
| I <sub>QBS</sub>   | Quiescent V <sub>BS</sub> supply current                             | —    | 30   | 55   |       | V <sub>IN</sub> = 0V or 5V                                        |
| I <sub>QCC</sub>   | Quiescent V <sub>CC</sub> supply current                             | —    | 150  | 270  |       | V <sub>IN</sub> = 0V or 5V                                        |
| I <sub>IN+</sub>   | Logic "1" input bias current                                         | —    | 3    | 10   |       | V <sub>IN</sub> = 5V (IR2101)<br>V <sub>IN</sub> = 0V (IR2102)    |
| I <sub>IN-</sub>   | Logic "0" input bias current                                         | —    | —    | 1    |       | V <sub>IN</sub> = 0V (IR2101)<br>V <sub>IN</sub> = 5V (IR2102)    |
| V <sub>CCUV+</sub> | V <sub>CC</sub> supply undervoltage positive going threshold         | 8    | 8.9  | 9.8  | V     |                                                                   |
| V <sub>CCUV-</sub> | V <sub>CC</sub> supply undervoltage negative going threshold         | 7.4  | 8.2  | 9    |       |                                                                   |
| I <sub>O+</sub>    | Output high short circuit pulsed current                             | 130  | 210  | —    | mA    | V <sub>O</sub> = 0V<br>V <sub>IN</sub> = Logic "1"<br>PW ≤ 10 μs  |
| I <sub>O-</sub>    | Output low short circuit pulsed current                              | 270  | 360  | —    |       | V <sub>O</sub> = 15V<br>V <sub>IN</sub> = Logic "0"<br>PW ≤ 10 μs |

# IR2101/IR2102 (S)

International  
**IR** Rectifier

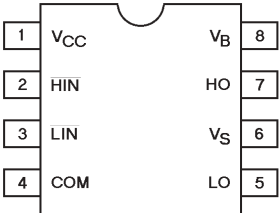
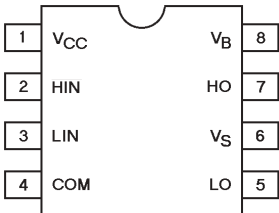
## Functional Block Diagram

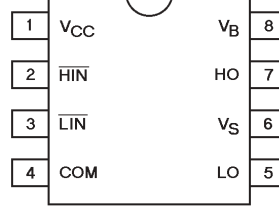
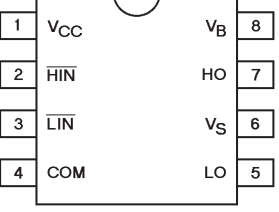


**Lead Definitions**

| Symbol                  | Description                                                              |
|-------------------------|--------------------------------------------------------------------------|
| HIN                     | Logic input for high side gate driver output (HO), in phase (IR2101)     |
| $\overline{\text{HIN}}$ | Logic input for high side gate driver output (HO), out of phase (IR2102) |
| LIN                     | Logic input for low side gate driver output (LO), in phase (IR2101)      |
| $\overline{\text{LIN}}$ | Logic input for low side gate driver output (LO), out of phase (IR2102)  |
| V <sub>B</sub>          | High side floating supply                                                |
| HO                      | High side gate drive output                                              |
| V <sub>S</sub>          | High side floating supply return                                         |
| V <sub>CC</sub>         | Low side and logic fixed supply                                          |
| LO                      | Low side gate drive output                                               |
| COM                     | Low side return                                                          |

**Lead Assignments**

|                                                                                                                             |                                                                                                                               |
|-----------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|
|  <p>8 Lead PDIP</p> <p><b>IR2101</b></p> |  <p>8 Lead SOIC</p> <p><b>IR2101S</b></p> |
|-----------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|

|                                                                                                                             |                                                                                                                               |
|-----------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|
|  <p>8 Lead PDIP</p> <p><b>IR2102</b></p> |  <p>8 Lead SOIC</p> <p><b>IR2102S</b></p> |
|-----------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|

# IR2101/IR2102 (S)

International  
**IR** Rectifier

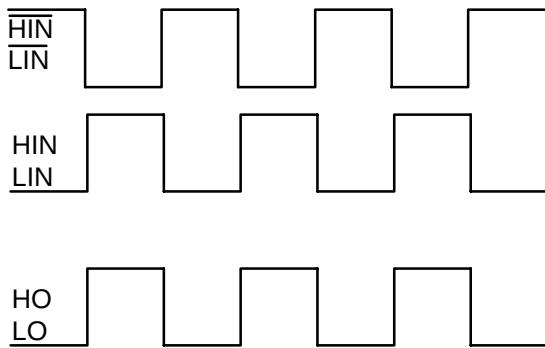


Figure 1. Input/Output Timing Diagram

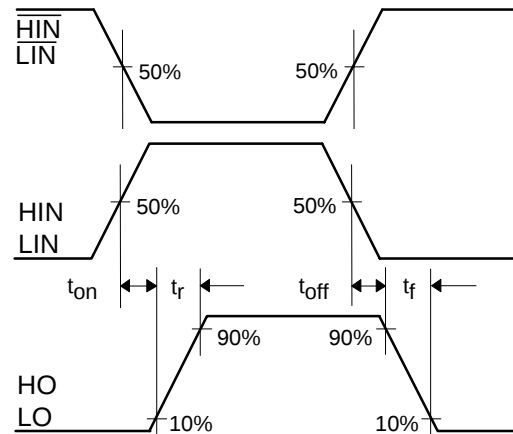


Figure 2. Switching Time Waveform Definitions

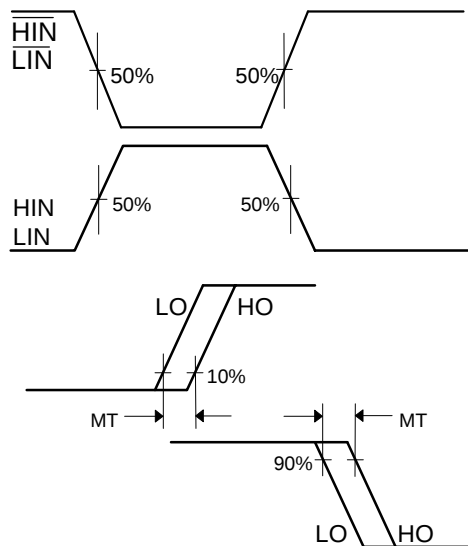
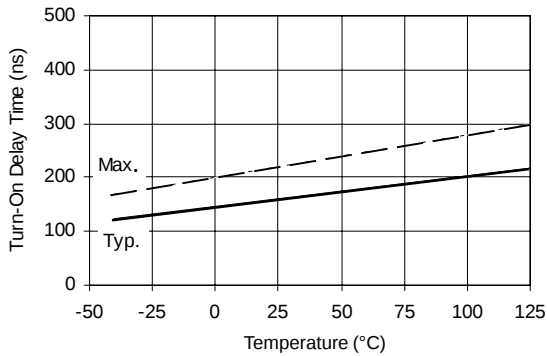
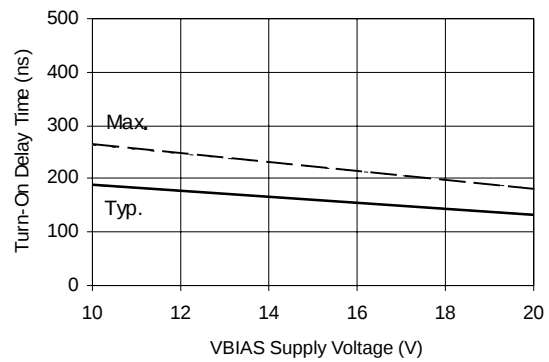


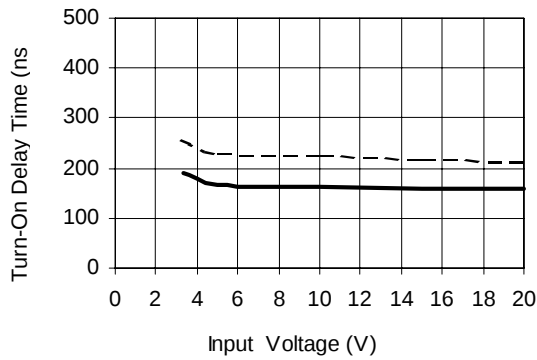
Figure 3. Delay Matching Waveform Definitions



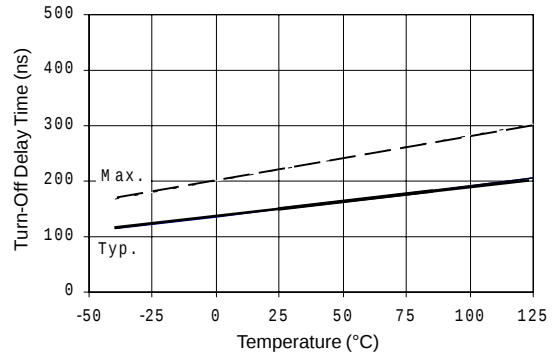
**Figure 6A. Turn-On Time vs Temperature**



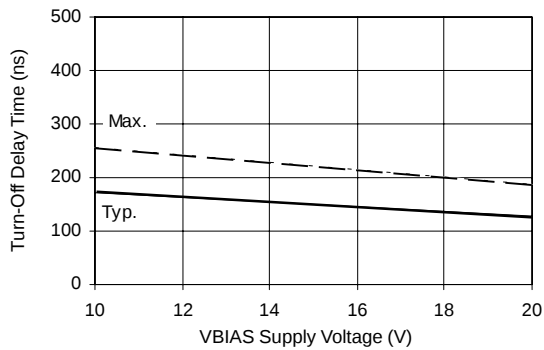
**Figure 6B. Turn-On Time vs Supply Voltage**



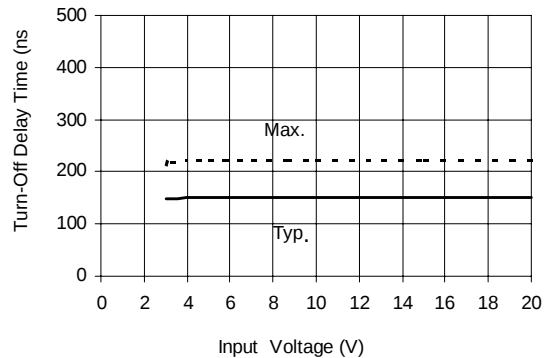
**Figure 6C. Turn-On Time vs Input Voltage**



**Figure 7A. Turn-Off Time vs Temperature**



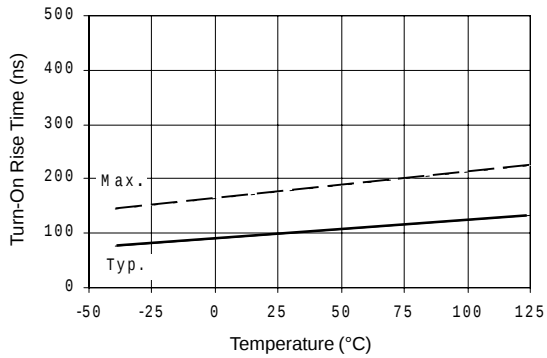
**Figure 7B. Turn-Off Time vs Supply Voltage**



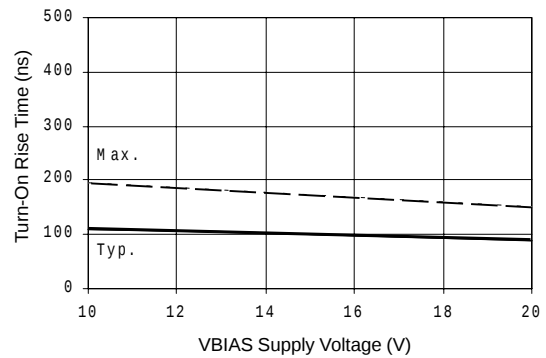
**Figure 7C. Turn-Off Time vs Input Voltage**

# IR2101/IR2102 (S)

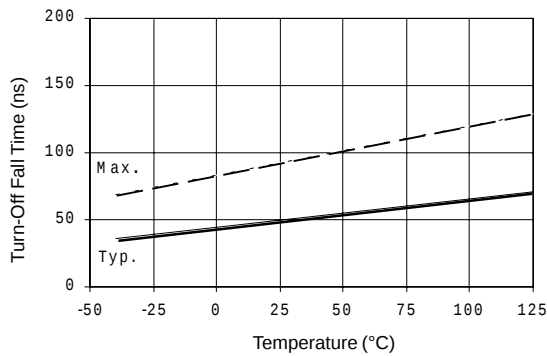
International  
**IR** Rectifier



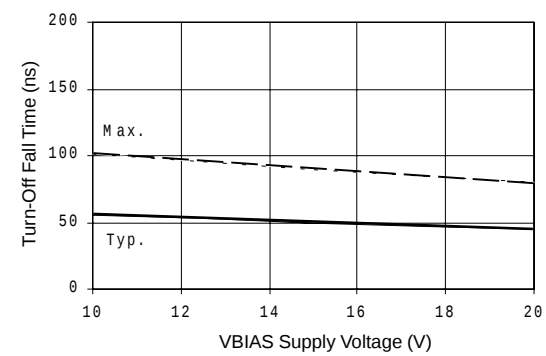
**Figure 9A. Turn-On Rise Time vs Temperature**



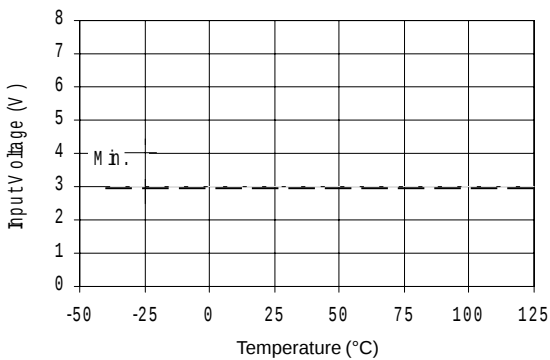
**Figure 9B. Turn-On Rise Time vs Voltage**



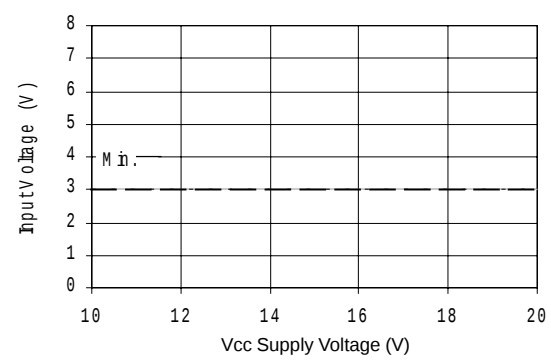
**Figure 10A. Turn-Off Fall Time vs Temperature**



**Figure 10B. Turn-Off Fall Time vs Voltage**

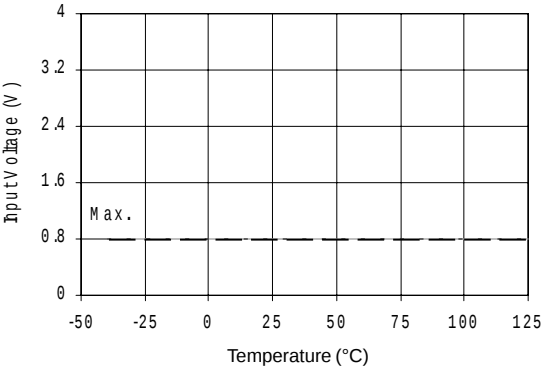


**Figure 12A. Logic "1" Input Voltage (IR2101)  
Logic "0" Input Voltage (IR2102)  
vs Temperature**

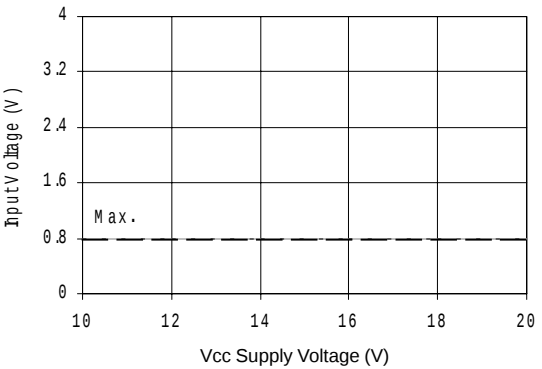


**Figure 12B. Logic "1" Input Voltage (IR2101)  
Logic "0" Input Voltage (IR2102)  
vs Voltage**

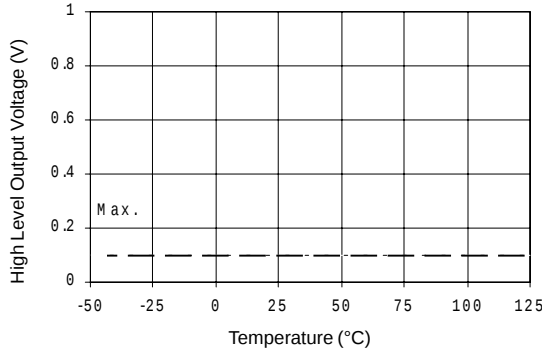
**IR2101/IR2102 (S)**



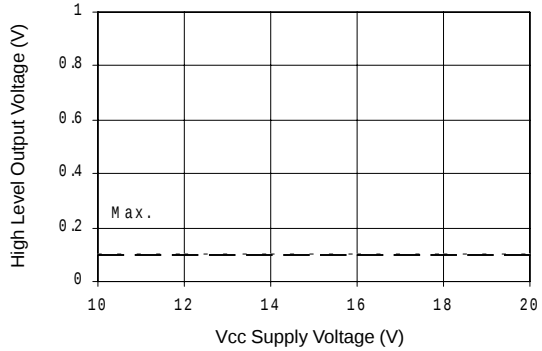
**Figure 13A. Logic "0" Input Voltage (IR2101)  
Logic "1" Input Voltage (IR2102)  
vs Temperature**



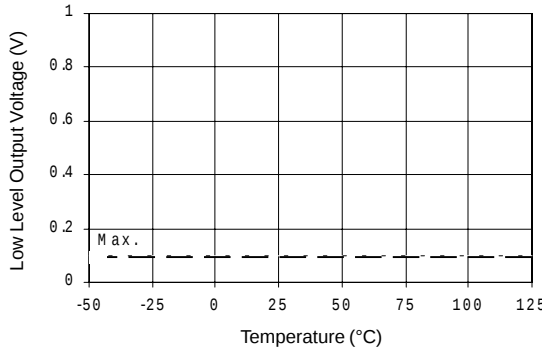
**Figure 13B. Logic "0" Input Voltage (IR2101)  
Logic "1" Input Voltage (IR2102)  
vs Voltage**



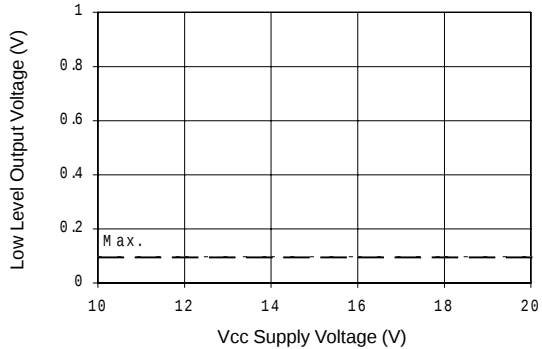
**Figure 14A. High Level Output  
vs Temperature**



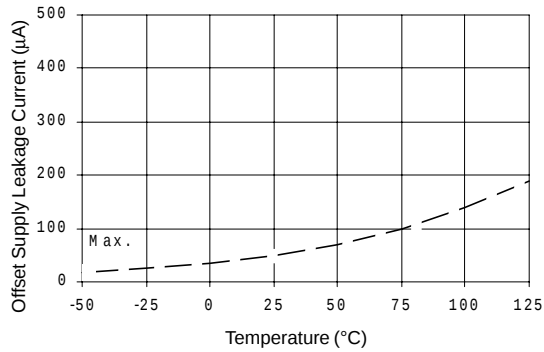
**Figure 14B. High Level Output vs Voltage**



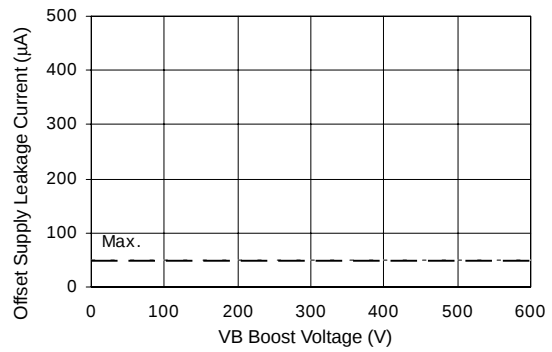
**Figure 15A. Low Level Output  
vs Temperature**



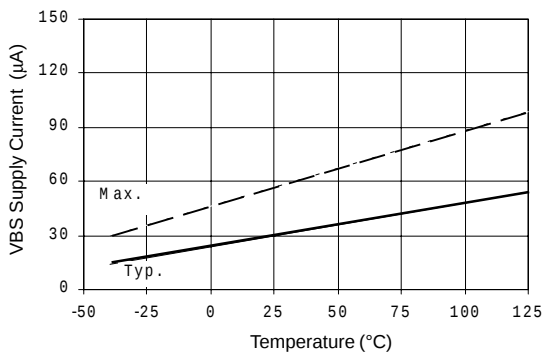
**Figure 15B. Low level Output vs Voltage**



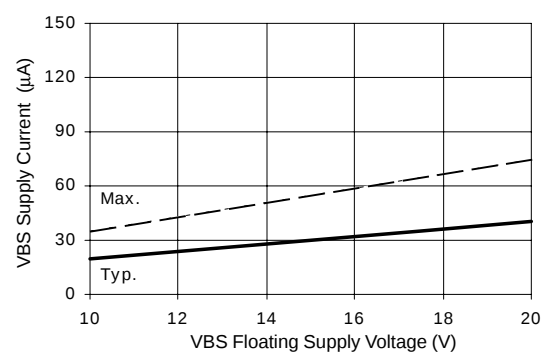
**Figure 16A. Offset Supply Current vs Temperature**



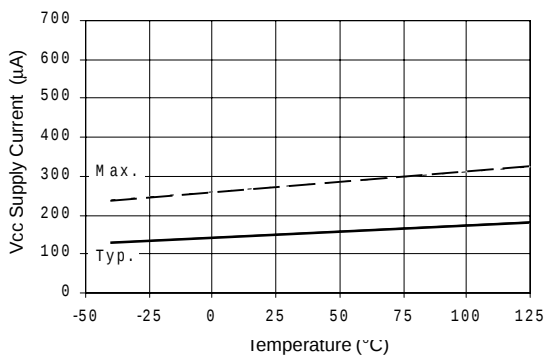
**Figure 16B. Offset Supply Current vs Voltage**



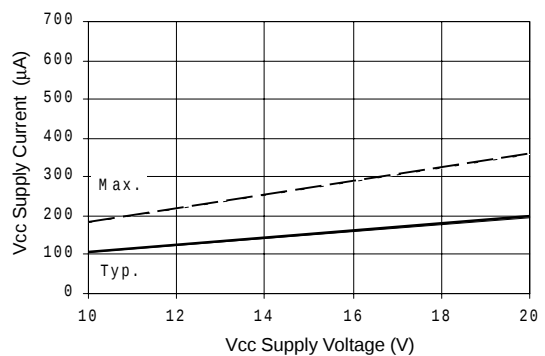
**Figure 17A. V<sub>BS</sub> Supply Current vs Temperature**



**Figure 17B. V<sub>BS</sub> Supply Current vs Voltage**

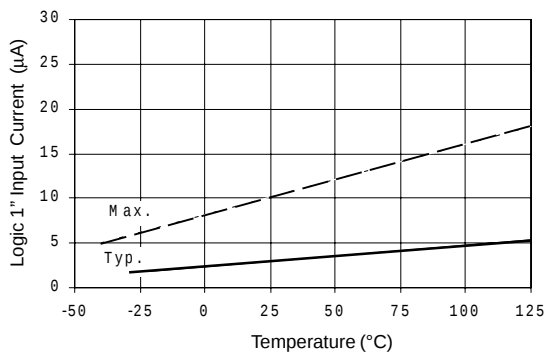


**Figure 18A. V<sub>CC</sub> Supply Current vs Temperature**

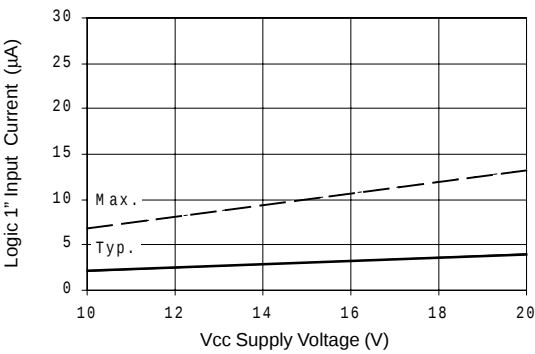


**Figure 18B. V<sub>CC</sub> Supply Current vs Voltage**

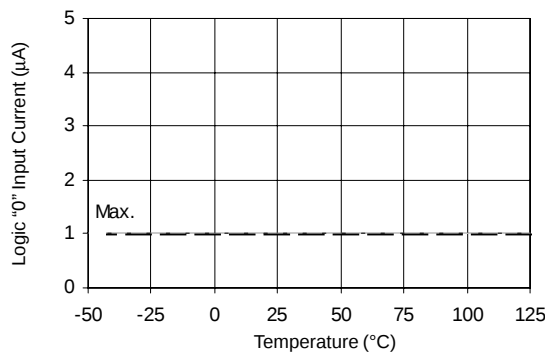
**IR2101/IR2102 (S)**



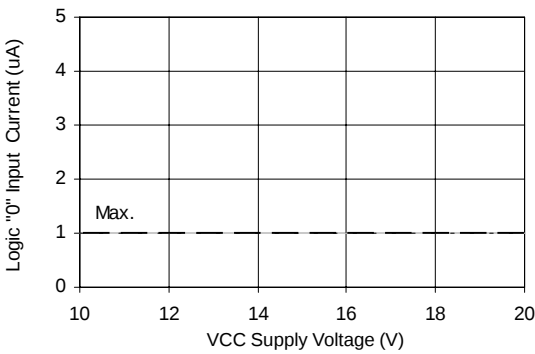
**Figure 19A. Logic "1" Input Current vs Temperature**



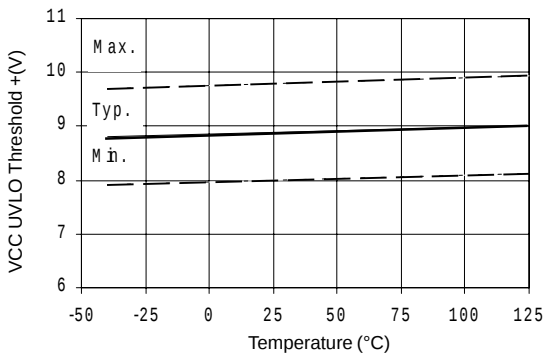
**Figure 19B. Logic "1" Input Current vs Voltage**



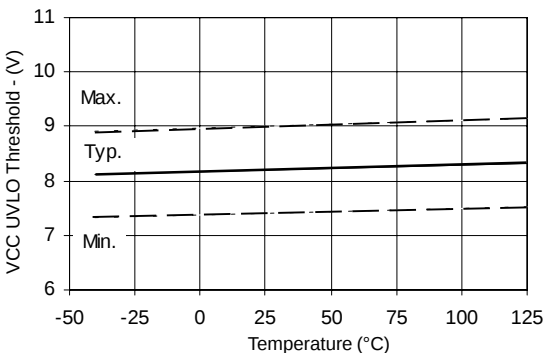
**Figure 20A. Logic "0" Input Current vs Temperature**



**Figure 20B. Logic "0" Input Current vs Voltage**



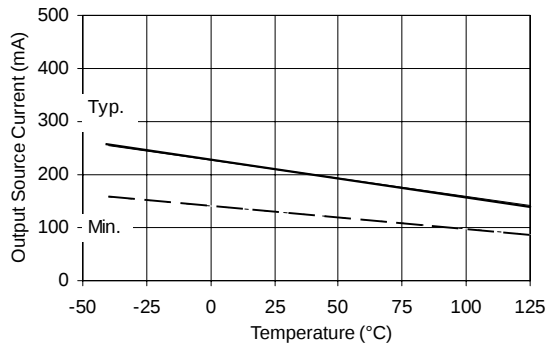
**Figure 21A. Vcc Undervoltage Threshold(+) vs Temperature**



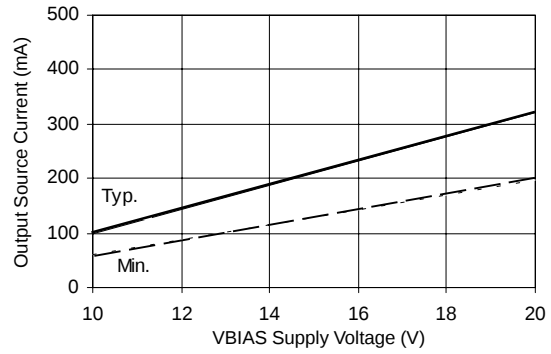
**Figure 21B. Vcc Undervoltage Threshold(-) vs Temperature**

# IR2101/IR2102 (S)

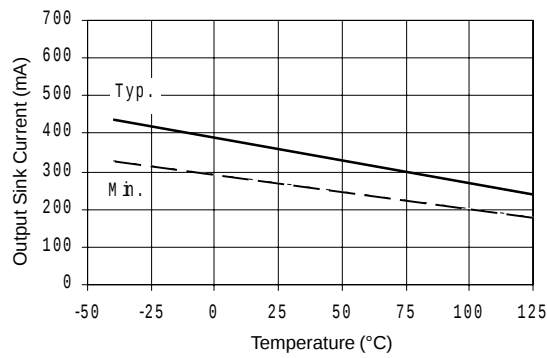
International  
**IR** Rectifier



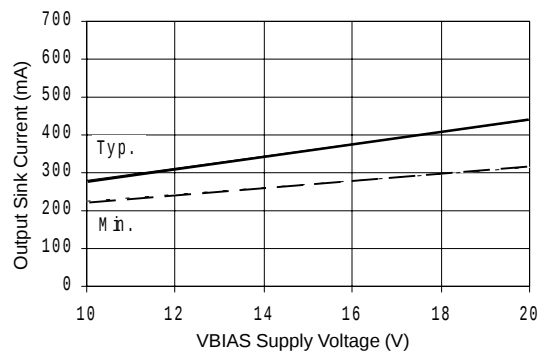
**Figure 22A. Output Source Current vs Temperature**



**Figure 22B. Output Source Current vs Voltage**

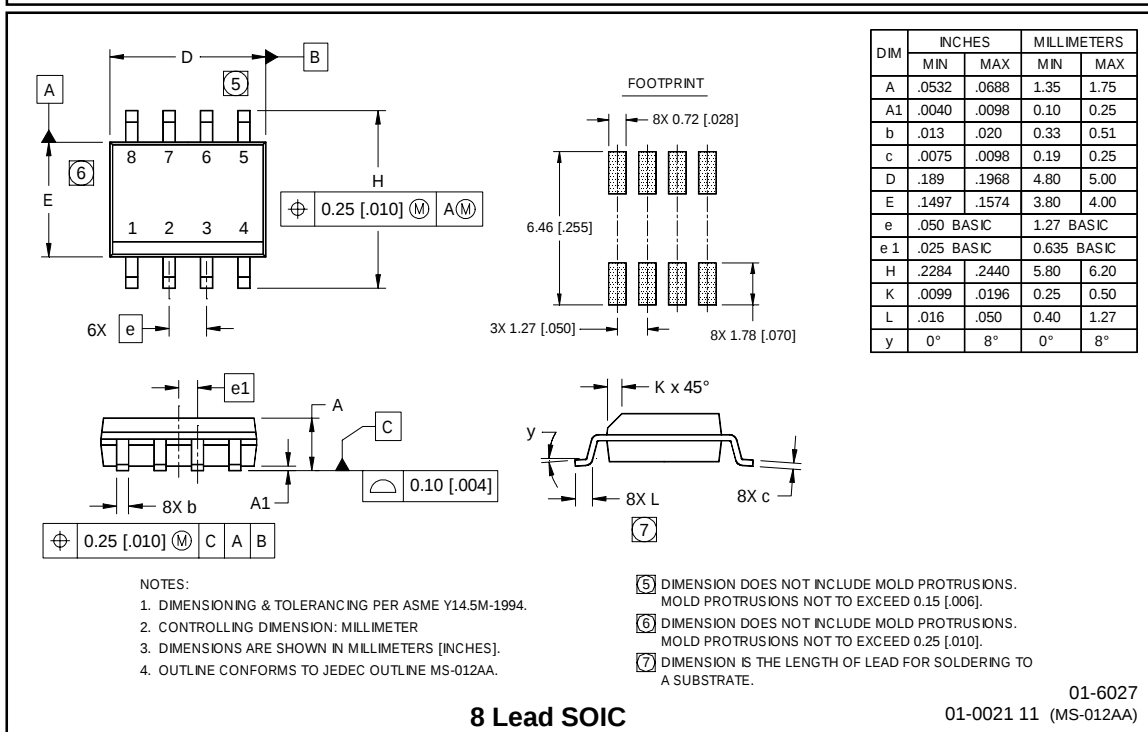
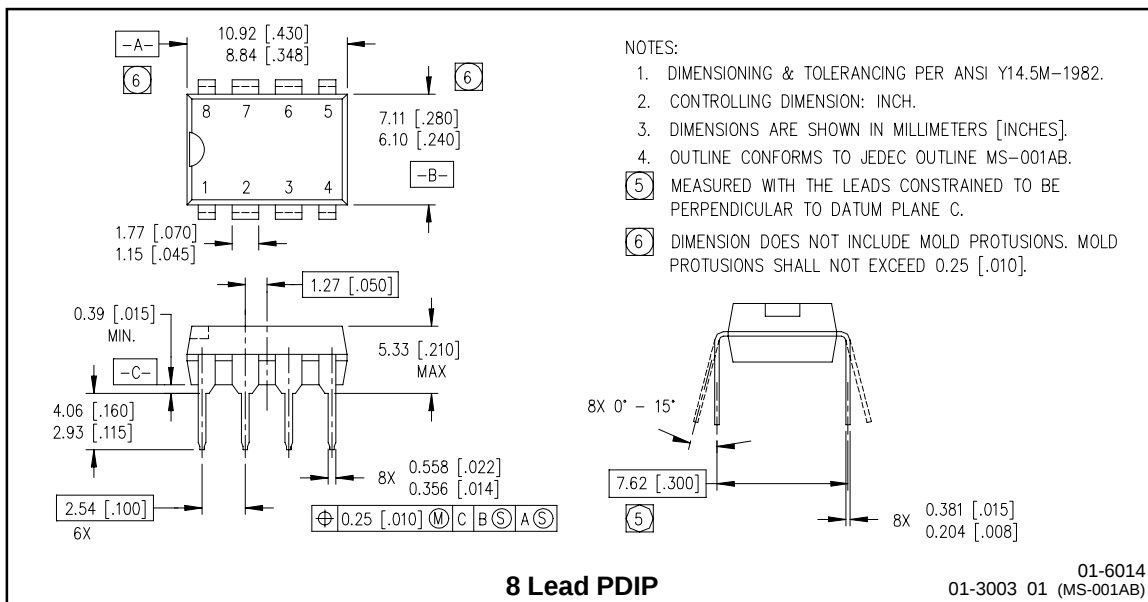


**Figure 23A. Output Sink Current vs Temperature**



**Figure 23B. Output Sink Current vs Voltage**

## Case outlines



IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105  
Data and specifications subject to change without notice. 4/18/2003