

IR2117/IR2118

SINGLE CHANNEL DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- CMOS Schmitt-triggered inputs with pull-down
- Output in phase with input (IR2117) or out of phase with input (IR2118)

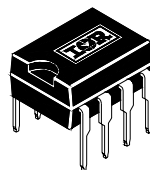
Description

The IR2117/IR2118 is a high voltage, high speed power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS outputs. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high or low side configuration which operates up to 600 volts.

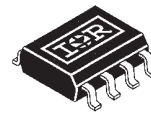
Product Summary

V_{OFFSET}	600V max.
$I_{\text{O+/-}}$	200 mA / 420 mA
V_{OUT}	10 - 20V
$t_{\text{on/off (typ.)}}$	125 & 105 ns

Packages

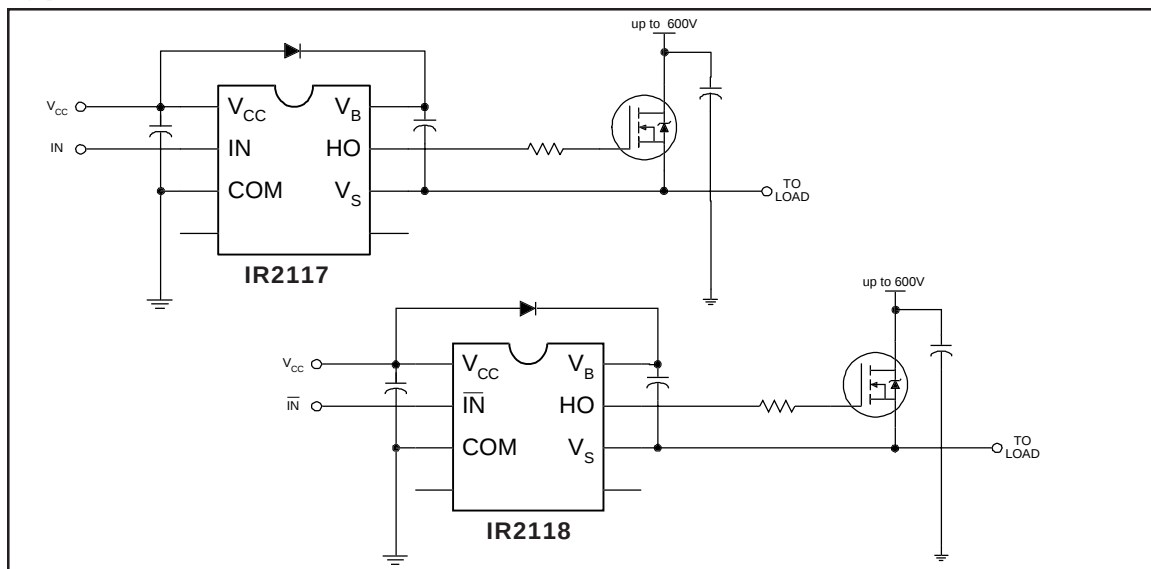


8 Lead PDIP
IR2117/IR2118



8 Lead SOIC
IR2117S/IR2118S

Typical Connection



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 5 through 8.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	-0.3	625	V
V_S	High side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$	
V_{HO}	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
V_{CC}	Logic supply voltage	-0.3	25	
V_{IN}	Logic input voltage	-0.3	$V_{CC} + 0.3$	
dV_S/dt	Allowable offset supply voltage transient (figure 2)	—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25^\circ\text{C}$ (8 lead PDIP)	—	1.0	W
	(8 lead SOIC)	—	0.625	
R_{thJA}	Thermal resistance, junction to ambient (8 lead PDIP)	—	125	$^\circ\text{C/W}$
	(8 lead SOIC)	—	200	
T_J	Junction temperature	—	150	$^\circ\text{C}$
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Logic supply voltage	10	20	
V_{IN}	Logic input voltage	0	V_{CC}	
T_A	Ambient temperature	-40	125	$^\circ\text{C}$

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	125	200	ns	$V_S = 0V$
t_{off}	Turn-off propagation delay	—	105	180		$V_S = 600V$
t_r	Turn-on rise time	—	80	130		
t_f	Turn-off fall time	—	40	65		

Static Electrical Characteristics

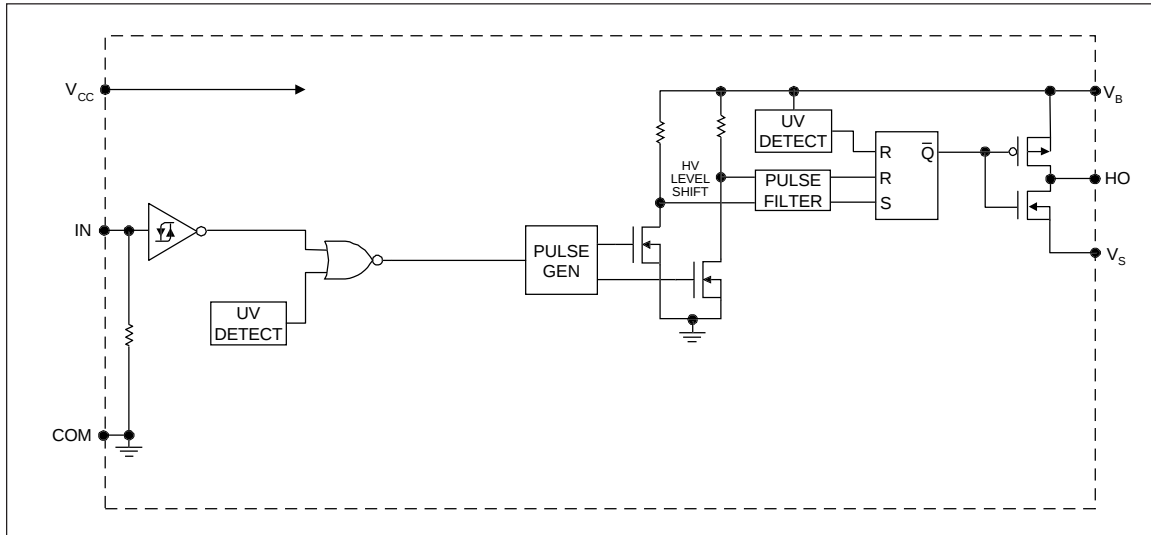
V_{BIAS} (V_{CC} , V_{BS}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	input voltage - logic "1" (IR2117) logic "0" (IR2118)	9.5	—	—	V	
V_{IL}	Input voltage - logic "0" (IR2117) logic "1" (IR2118)	—	—	6.0		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	—	100	mV	$I_O = 0A$
V_{OL}	Low level output voltage, V_O	—	—	100		$I_O = 0A$
I_{LK}	Offset supply leakage current	—	—	50	μA	$V_B = V_S = 600V$
I_{QBS}	Quiescent V_{BS} supply current	—	50	240		$V_{IN} = 0V$ or V_{CC}
I_{QCC}	Quiescent V_{CC} Supply Current	—	70	340		$V_{IN} = 0V$ or V_{CC}
I_{IN+}	Logic "1" input bias current (IR2117)	—	20	40		$V_{IN} = V_{CC}$
	(IR2118)					$V_{IN} = 0V$
I_{IN-}	Logic "0" input bias current (IR2117)	—	—	1.0		$V_{IN} = 0V$
	(IR2118)					$V_{IN} = V_{CC}$
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	7.6	8.6	9.6	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.2	8.2	9.2		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	7.6	8.6	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.2	8.2	9.2		
I_{O+}	Output high short circuit pulsed current	200	250	—	mA	$V_O = 0V$ $V_{IN} = \text{Logic "1"}$ $PW \leq 10 \mu s$
I_{O-}	Output low short circuit pulsed current	420	500	—		$V_O = 15V$ $V_{IN} = \text{Logic "0"}$ $PW \leq 10 \mu s$

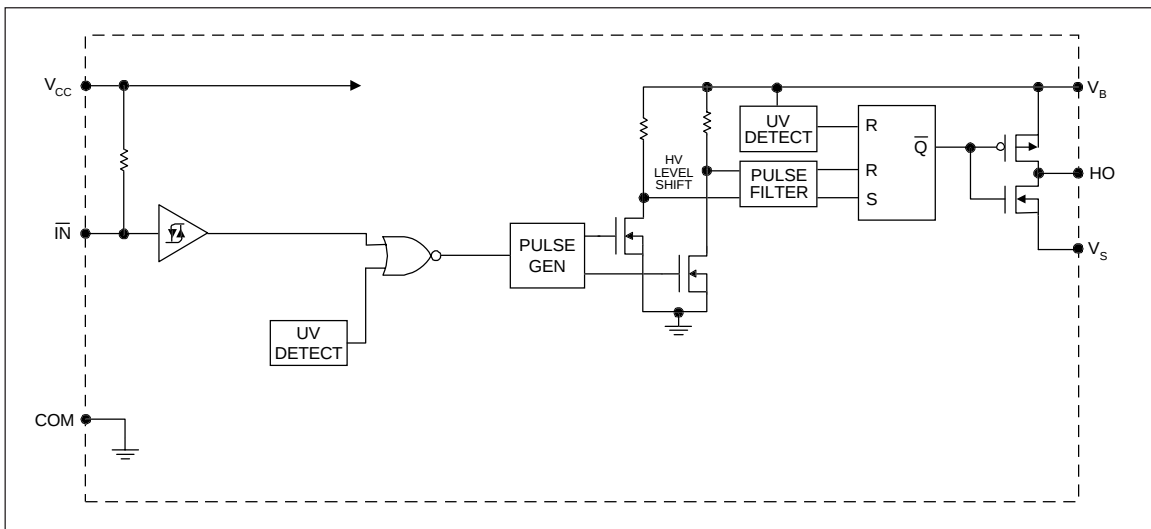
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Functional Block Diagram (IR2117)



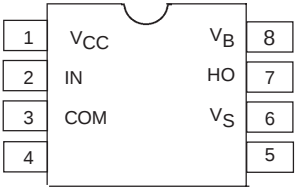
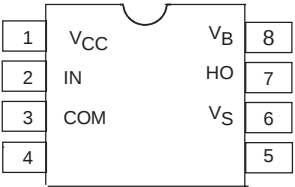
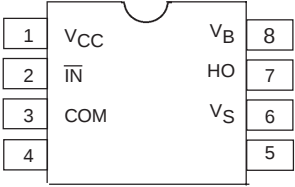
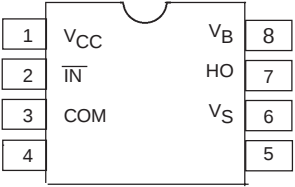
Functional Block Diagram (IR2118)



Lead Definitions

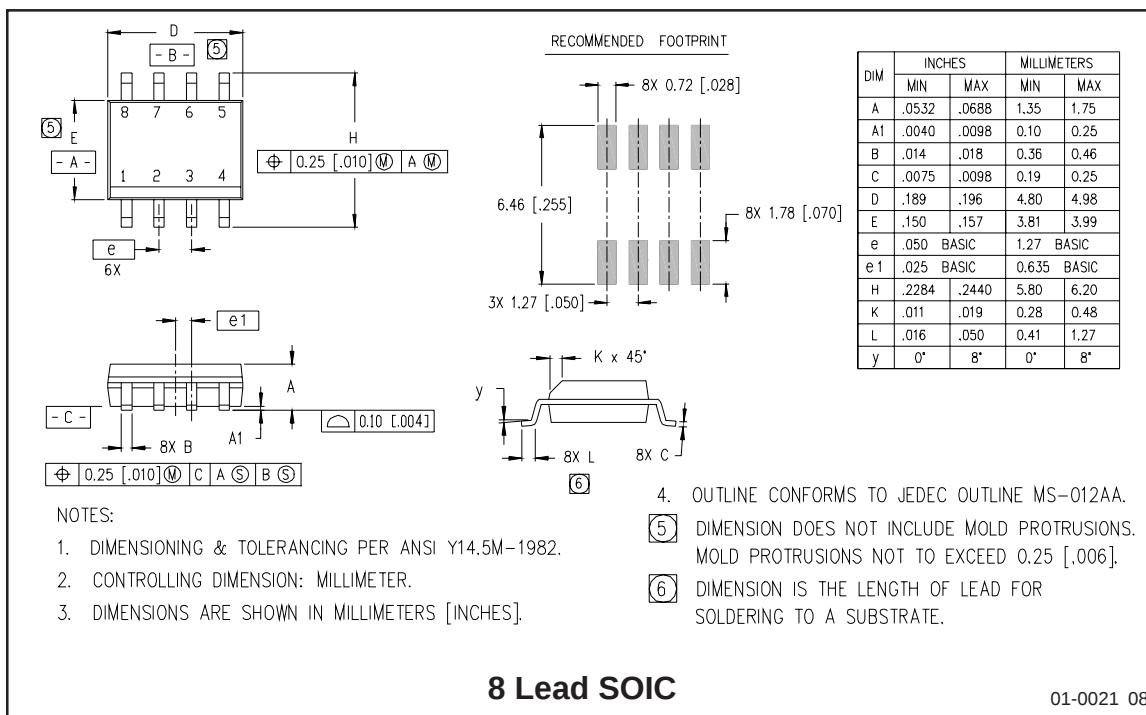
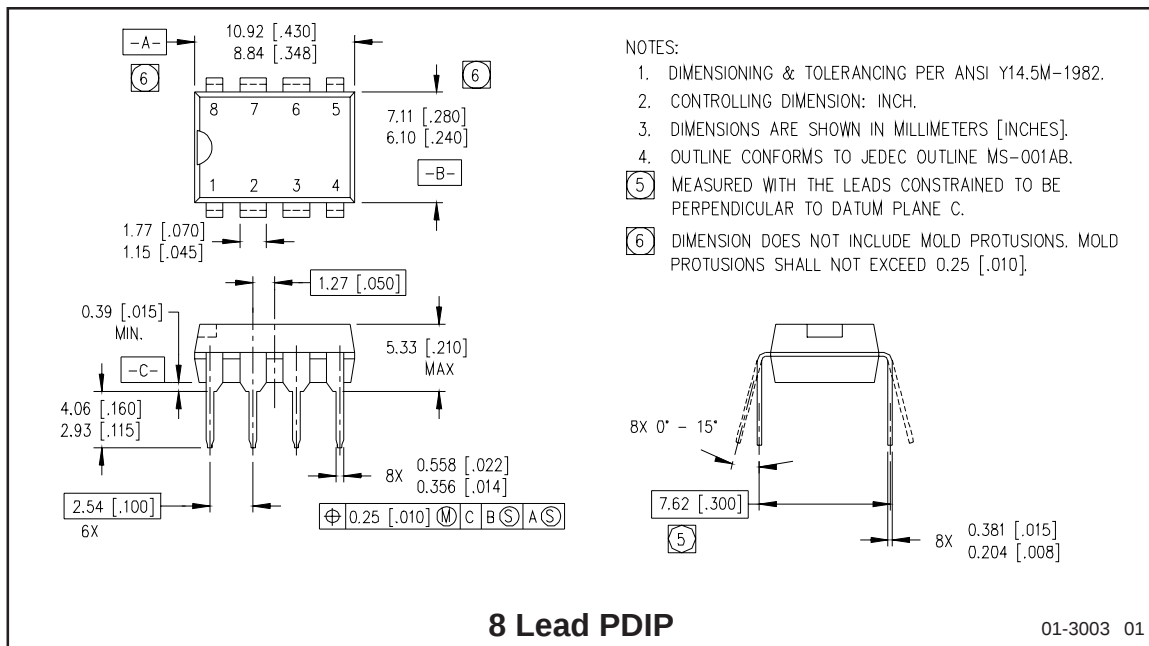
Symbol	Description
V _{CC}	Logic and gate drive supply
IN	Logic input for gate driver output (HO), in phase with HO (IR2117)
$\overline{\text{IN}}$	Logic input for gate driver output (HO), out of phase with HO (IR2118)
COM	Logic ground
V _B	High side floating supply
HO	High side gate drive output
V _S	High side floating supply return

Lead Assignments

 8 Lead PDIP IR2117	 8 Lead SOIC IR2117S
 8 Lead PDIP IR2118	 8 Lead SOIC IR2118S

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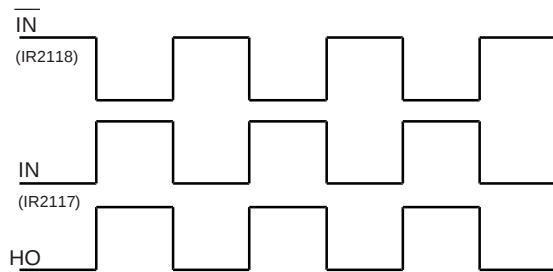


Figure 1. Input/Output Timing Diagram

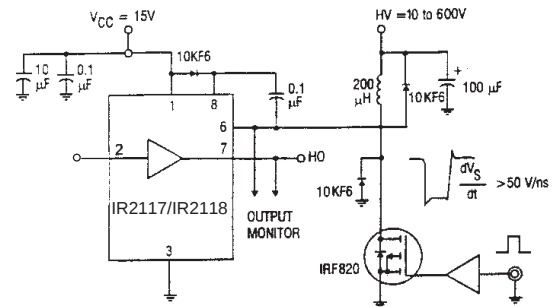


Figure 2. Floating Supply Voltage Transient Test Circuit

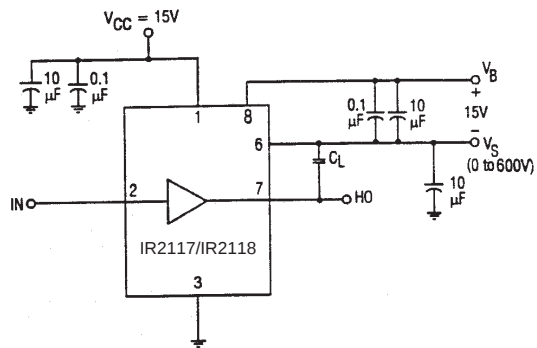


Figure 3. Switching Time Test Circuit

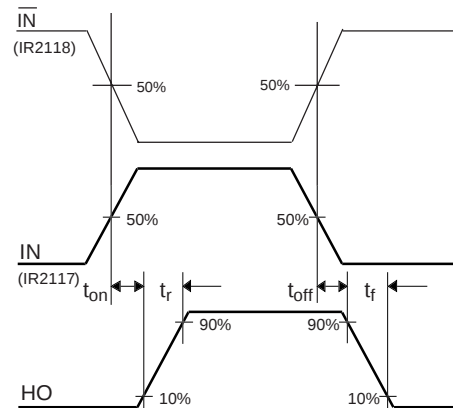


Figure 4. Switching Time Waveform Definition

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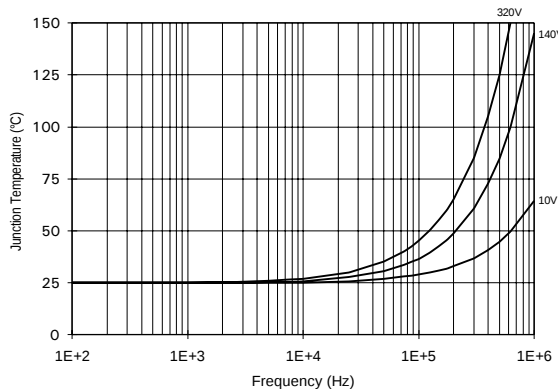


Figure 5. IR2117/IR2118 T_J vs. Frequency (IRFBC20)
 $R_{GATE} = 33\Omega$, $V_{CC} = 15V$

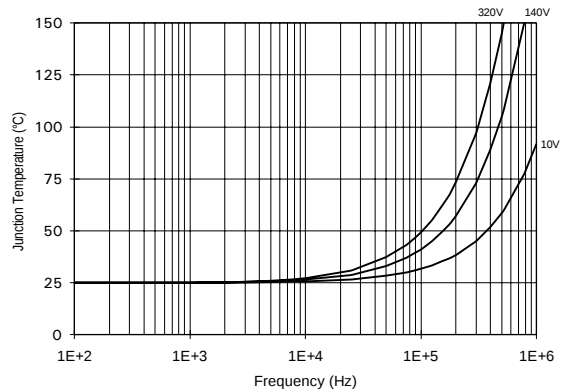


Figure 6. IR2117/IR2118 T_J vs. Frequency (IRFBC30)
 $R_{GATE} = 22\Omega$, $V_{CC} = 15V$

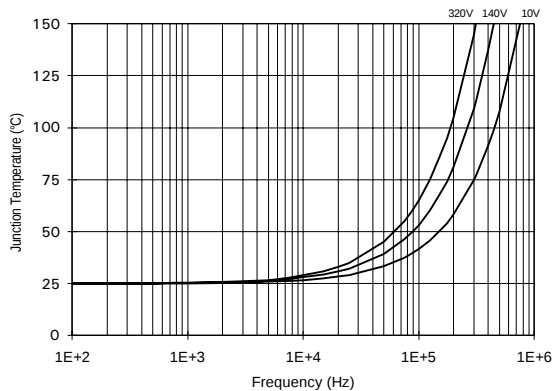


Figure 7. IR2117/IR2118 T_J vs. Frequency (IRFBC40)
 $R_{GATE} = 15\Omega$, $V_{CC} = 15V$

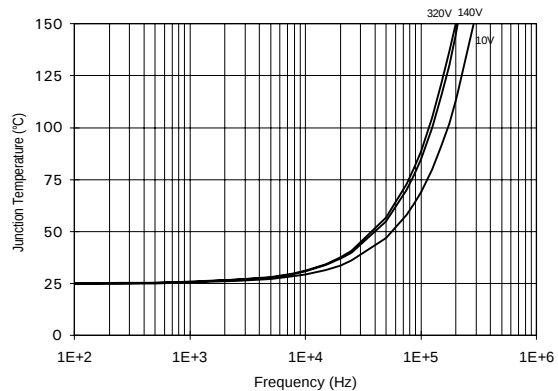


Figure 8. IR2117/IR2118 T_J vs. Frequency (IRFPE50)
 $R_{GATE} = 10\Omega$, $V_{CC} = 15V$

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WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 322 3331

IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020

IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T 3Z2 Tel: (905) 453-2200

IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590

IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111

IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171 Tel: 81 3 3983 0086

IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: 65 838 4630

IR TAIWAN: 16 Fl. Suite D..207, Sec.2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936

<http://www.irf.com/>

Data and specifications subject to change without notice. 3/1/99