



IRFK6HC50, IRFK6JC50

Isolated Base Power HEX-pak™ Assembly - Parallel Chip Configuration

- High Current Capability.
- UL recognised E78996.
- Electrically Isolated Base Plate.
- Easy Assembly into Equipment.



Description

The HEX-pak™ utilises the well-proven HEXFET™ die, combining low on-state resistance with high transconductance. These superior technology die are assembled by state of the art techniques into the TO-240 package, featuring 2.5kV rms isolation and solid M5 screw connections. The small footprint means the package is highly suited to power applications where space is a premium. Available in two versions, IRFK.H... for fast switching and IRFK.J... for oscillation sensitive applications.

$$V_{DS} = 600V$$

$$R_{DS(on)} = 100m\Omega$$

$$I_D = 48A$$

Absolute Maximum Rating

	Parameter	Max.	Units
I_D @ $T_C=25^\circ C$	Continuous Drain Current	48	A
I_D @ $T_C=100^\circ C$	Continuous Drain Current	30	A
I_{DM}	Pulse Drain Current	192	A ①
P_D @ $T_C=25^\circ C$	Maximum Power Dissipation	625	W
V_{GS}	Gate-to-Source Voltage	20	V
V_{INS}	R.M.S. Isolation Voltage, circuit to base	2.5	kV
T_J	Operating Junction Temperature Range	-40 to 150	$^\circ C$
T_{STG}	Storage Temperature Range	-40 to 150	$^\circ C$

Thermal and Mechanical Specifications

	Parameter	Min.	Typ.	Max.	Units
R_{thJC}	Junction-to-Case	-	-	0.20	K/W ②
R_{thCS}	Case-to-Sink, smooth & greased surface	-	0.1	-	K/W
T	Mounting Torque +10%				③
	HEXpak to Heatsink	-	5	-	Nm
	Busbar to HEXpak	-	3	-	Nm
wt	Approximate Weight	-	140	-	g
		-	5	-	oz

Notes:

① - Repetitive Rating: Pulse width limited by maximum junction temperature see figure 8.

② - Per Module.

③ - A mounting compound is recommended and the torque should be rechecked after a period of three hours to allow for the spread of the compound.

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Electrical Characteristics @ $T_J = 25^{\circ}\text{C}$ (Unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
B_{VDS}	Drain-to-Source Breakdown voltage	600	-	-	V	$V_{GS}=0V, I_D=1.0mA$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	-	80	100	m Ω	$V_{GS}=10V, I_D=30A$
$I_{D(on)}$	On-State Drain Current	48	-	-	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}^{max}, V_{GS}=10V$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	-	4.0	V	$V_{DS}=V_{GS}, I_D=1.5mA$
g_{fs}	Forward Transconductance ④	35	53	-	S	$V_{DS} > 50V, I_D=30A$
I_{DSS}	Zero Gate Voltage Drain Current	-	-	1.5	mA	$V_{DS}=V_{DS}^{max}, V_{GS}=0V$
		-	-	6.0	mA	$V_{GS}=10V, T_C=125^{\circ}\text{C}, V_{DS}=V_{DS}^{max} \times 0.8$
I_{GSS}	Gate-to-Source Leakage Forward	-	-	600	nA	$V_{GS}=20V$
I_{GSS}	Gate-to-Source Leakage Reverse	-	-	-600	nA	$V_{GS}=-20V$
Q_g	Total Gate Charge	-	720	780	nC	$I_D=48A, V_{GS}=10V,$
Q_{gs}	Gate-to-Source Charge	-	75	120	nC	$V_{DS}=V_{DS}^{max} \times 0.8$
Q_{gd}	Gate-to-Drain ("Miller") Charge	-	250	360	nC	
$t_{d(on)}$	Turn-on Delay Time	IRFK6HC50	-	80	-	$V_{DD}=300V, I_D=30A,$
		IRFK6JC50	-	90	-	
t_r	Rise Time	IRFK6HC50	-	60	-	$V_{GS}=10V,$
		IRFK6JC50	-	75	-	
$t_{d(off)}$	Turn-off Delay Time	IRFK6HC50	-	400	-	$R_{SOURCE}=3.3\Omega$
		IRFK6JC50	-	550	-	
t_f	Fall Time	IRFK6HC50	-	70	-	
		IRFK6JC50	-	110	-	
L_{DS}	Drain-to-Source Inductance	-	18	-	nH	
C_{iss}	Input Capacitance	-	14.0	-	nF	$V_{GS}=0V, V_{DS}=25V,$
C_{oss}	Output Capacitance	-	2.2	-	nF	$f=1.0MHz$
C_{rss}	Reverse Transfer Capacitance	-	1.0	-	nF	
	Linear Derating Factor	-	-	5	W/K	

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	-	-	48	A	
I_{SM}	Pulsed Source Current (Body Diode)	-	-	165	A	
V_{SD}	Diode Forward Voltage	-	-	1.8	V	$V_{GS}=0V, I_S=48A, T_C=25^{\circ}\text{C}$
t_{rr}	Reverse Recovery Time	370	770	1600	ns	$di/dt=400A/\mu s, T_J=150^{\circ}\text{C}$
Q_{rr}	Reverse Recovered Charge	19.0	38.0	78.0	μC	$I_S=48A$

Notes:

④ - Pulse Width $\leq 300\mu s$; Duty cycle $\leq 2\%$.

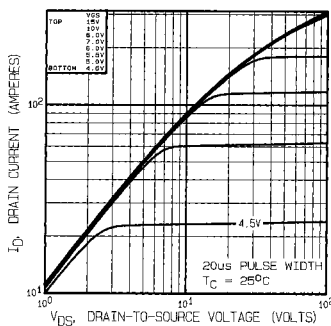


Fig 1. Typical Output Characteristics,
 $T_C = 25^\circ\text{C}$

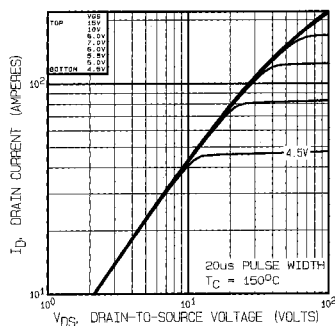


Fig 2. Typical Output Characteristics,
 $T_C = 150^\circ\text{C}$

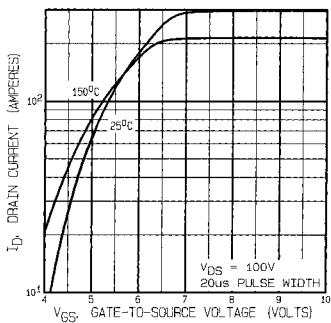


Fig 3. Typical Transfer Characteristics

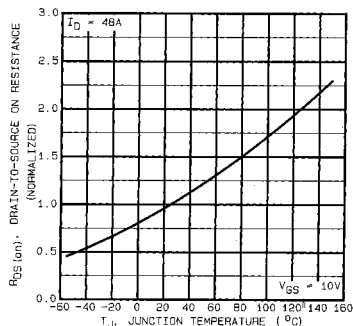


Fig 4. Normalized On-Resistance Vs.
Temperature

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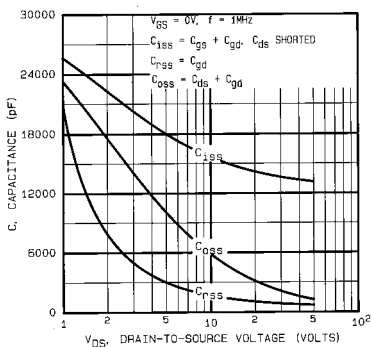


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

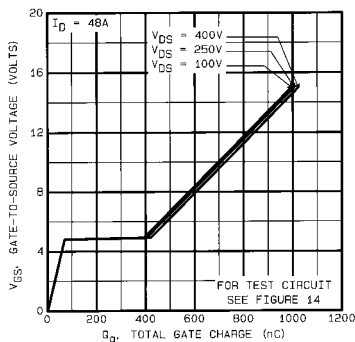


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

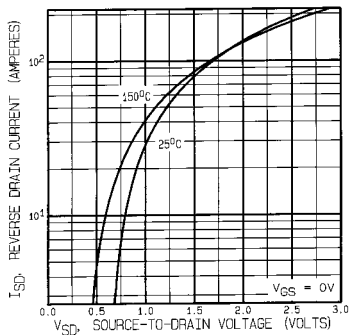


Fig 7. Typical Source-Drain Diode Forward Voltage

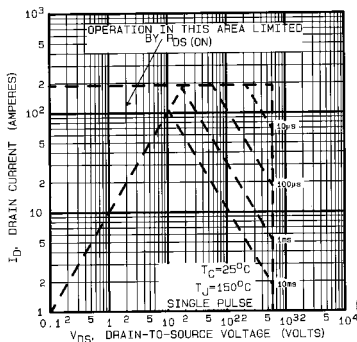


Fig 8. Maximum Safe Operating Area



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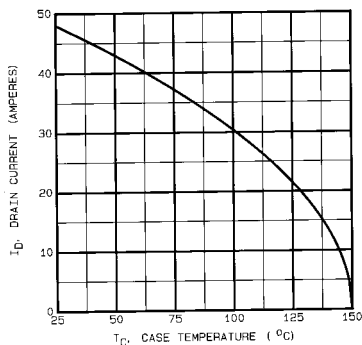


Fig 9. Maximum Drain Current Vs. Case Temperature

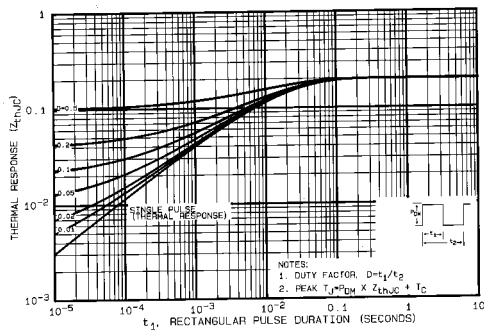


Fig 10. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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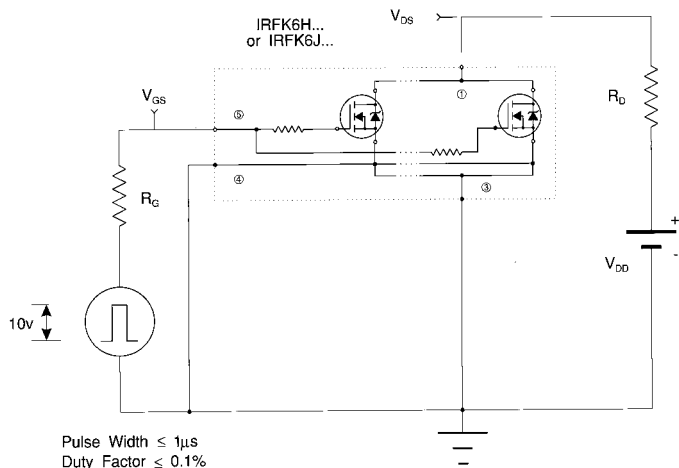


Fig 11a. Switching Time Test Circuit

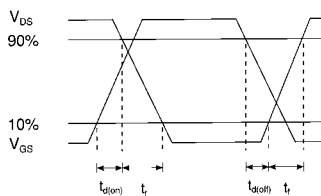
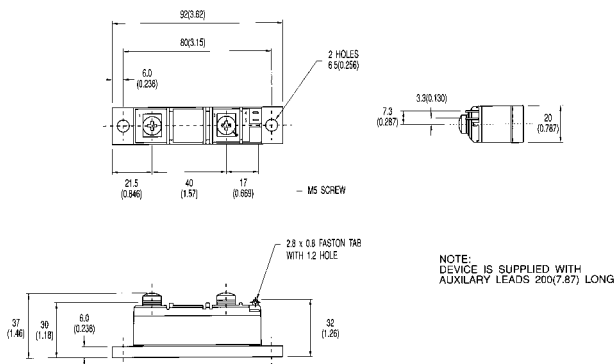
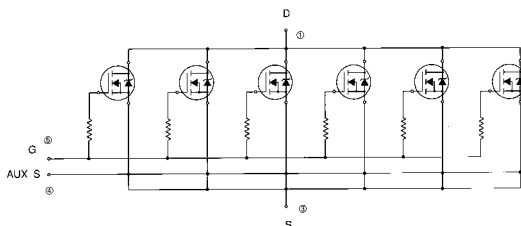


Fig 11b. Switching Time Waveforms



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Circuit Configuration and Outline

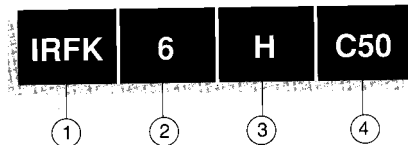


All dimensions in millimetres (inches)

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Part Numbering



1. - HEX-pak Module.
2. - Number of HEXFETs in parallel.
3. - H - Fast switching.
- J - Oscillation resistant for sensitive applications.
4. - Voltage code:-
054 - 60V
150 - 100V
250 - 200V
350 - 400V
450 - 500V
C50 - 600V

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