IRFP360, IRFP362

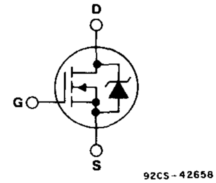
File Number **2290**

Avalanche-Energy-Rated N-Channel Power MOSFETs

23 A and 20 A, 400 V
$r_{DS(on)}$ = 0.20 Ω and 0.25 Ω

Features:
- *Single pulse avalanche energy rated*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*

N-CHANNEL ENHANCEMENT MODE

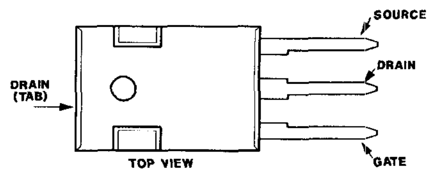


TERMINAL DIAGRAM

The IRFP360 and IRFP362 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

TERMINAL DESIGNATION



JEDEC TO-247

ABSOLUTE MAXIMUM RATINGS

Parameter		IRFP360	IRFP362	Units
I_D @ T_C = 25°C	Continuous Drain Current	23	20	A
I_D @ T_C = 100°C	Continuous Drain Current	14	13	A
I_{DM}	Pulsed Drain Current ①	92	80	A
P_D @ T_C = 25°C	Max. Power Dissipation	250		W
	Linear Derating Factor	2.0		W/°C
V_{GS}	Gate-to-Source Voltage	±20		V
E_{AS}	Single Pulse Avalanche Energy ②	1200 (See Fig. 14)		mJ
I_{AR}	Avalanche Current ①	23		A
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

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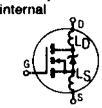
ELECTRICAL CHARACTERISTICS *At Case Temperature (T_J) = 25° C Unless Otherwise Specified*

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFP360 IRFP362	400	—	—	V	V_{GS} = 0V, I_D = 250μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRFP360	—	0.18	0.20	Ω	V_{GS} = 10V, I_D = 13A
		IRFP362	—	0.20	0.25		
$I_{D(on)}$	On-State Drain Current ③	IRFP360	23	—	—	A	V_{DS} > $I_{D(on)}$ × $R_{DS(on)}$ Max. V_{GS} = 10V
		IRFP362	20				
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance ③	ALL	14	21	—	S(℧)	V_{DS} ≥ 50V, I_{DS} = 13A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			—	—	1000		V_{DS} = 0.8 × Max. Rating, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-500	nA	V_{GS} = -20V
Q_g	Total Gate Charge	ALL	—	68	100	nC	V_{GS} = 10V, I_D = 25A
Q_{gs}	Gate-to-Source Charge	ALL	—	17	25	nC	V_{DS} = 0.8 × Max. Rating See Fig. 16
Q_{gd}	Gate-to-Drain ("Miller") Charge		—	24	36	nC	(Independent of operating temperature)
$t_{d(on)}$	Turn-On Delay Time	ALL	—	22	33	ns	V_{DD} = 200V, I_D = 25A, R_G = 4.3Ω
t_r	Rise Time	ALL	—	94	140	ns	R_D = 7.5Ω
$t_{d(off)}$	Turn-Off Delay Time	ALL	—	80	120	ns	See Fig. 15
t_f	Fall Time	ALL	—	66	99	ns	(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die. — Modified MOSFET symbol showing the internal inductances. 
L_S	Internal Source Inductance	ALL	—	13	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	—	4000	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	ALL	—	550	—	pF	f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	97	—	pF	See Fig. 10
R_{thJC}	Junction-to-Case	ALL	—	—	0.50	°C/W	
R_{thCS}	Case-to-Sink	ALL	—	0.24	—	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	—	—	40	°C/W	Typical socket mount
	Mounting torque	ALL	—	—	10	in.•lbs.	Standard 6-32 screw

① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 5) Refer to current HEXFET reliability report

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 4.0mH, R_G = 25Ω, Peak I_L = 23A

③ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

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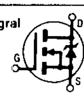
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	—	—	23	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier. 
I_{SM}	Pulsed Source Current (Body Diode) ①	ALL	—	—	92	A	
V_{SD}	Diode Forward Voltage ③	ALL	—	—	1.8	V	T_J = 25°C, I_S = 23A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	200	460	1000	ns	T_J = 25°C, I_F = 25A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	3.1	7.1	16	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

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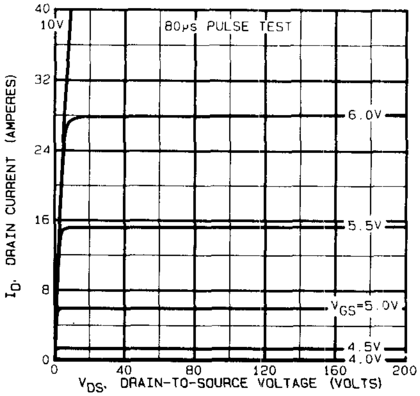

Fig. 1 - Typical output characteristics.

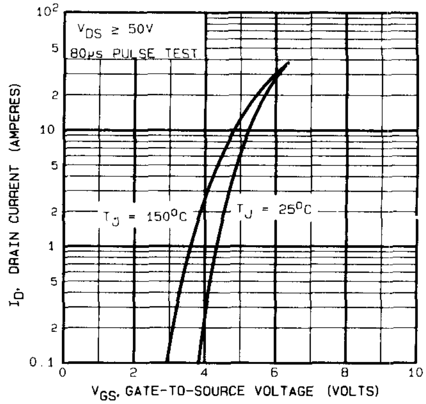

Fig. 2 - Typical transfer characteristics.

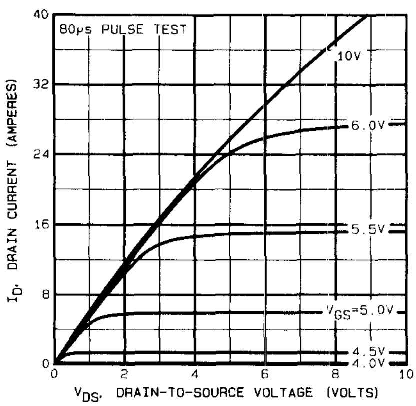

Fig. 3 - Typical saturation characteristics.

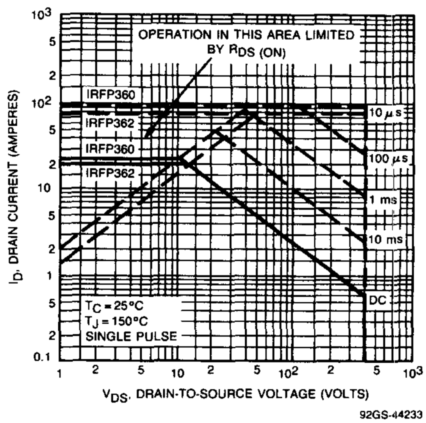

Fig. 4 - Maximum safe operating area.

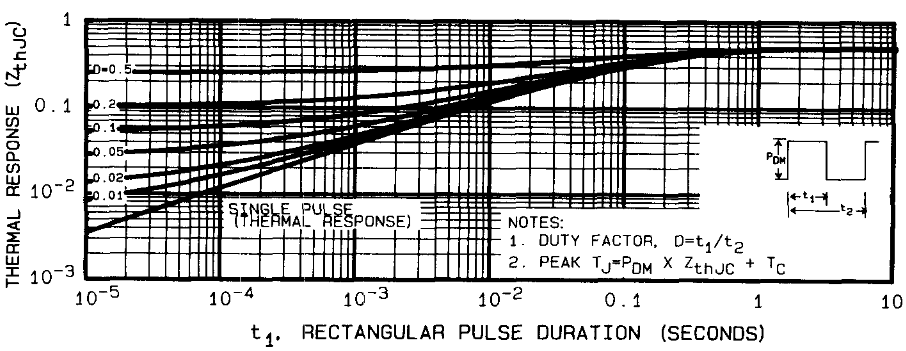

Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

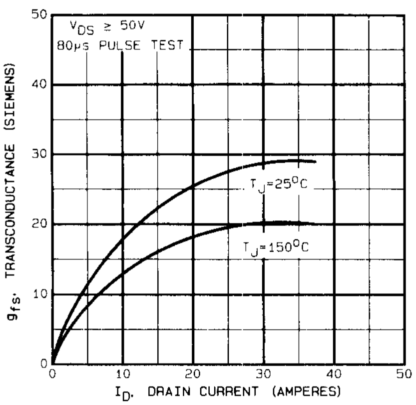

Fig. 6 - Typical transconductance vs. drain current.

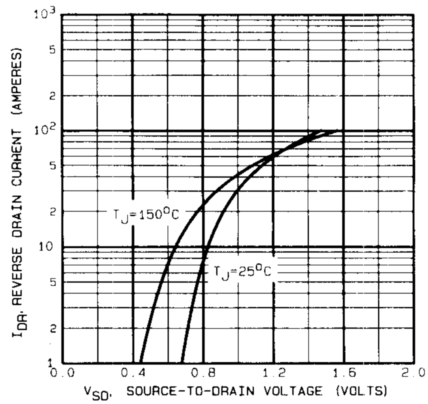

Fig. 7 - Typical source-drain diode forward voltage.

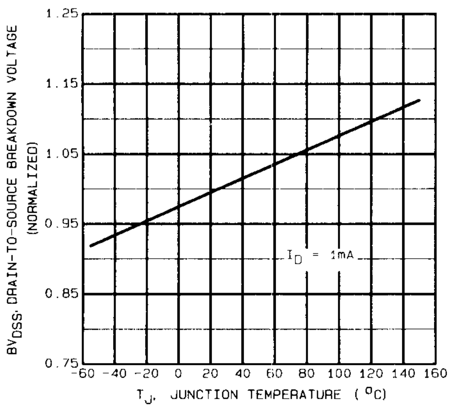

Fig. 8 - Breakdown voltage vs. temperature.

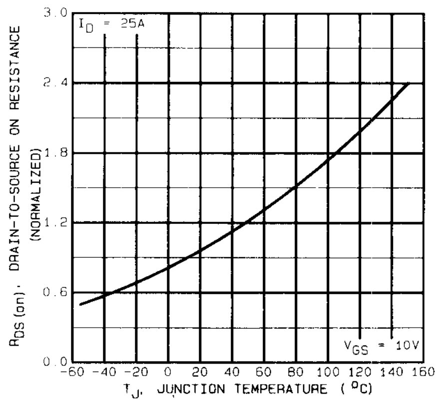

Fig. 9 - Normalized on-resistance vs. temperature.

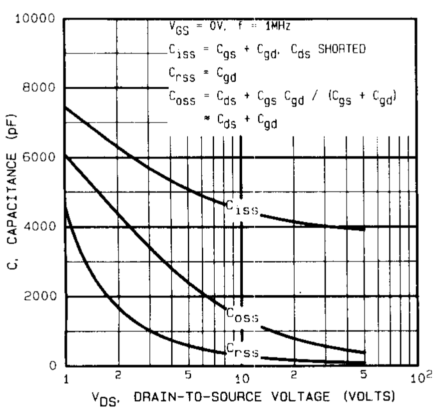

Fig. 10 - Typical capacitance vs. drain-to-source voltage.

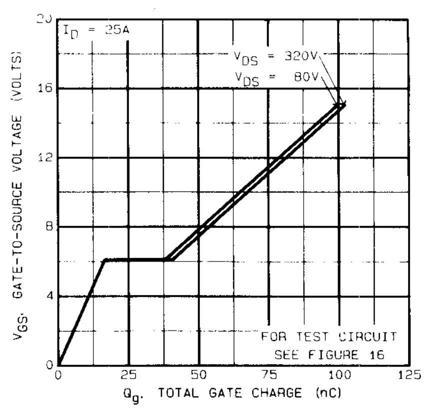

Fig. 11 - Typical gate charge vs. gate-to-source voltage.

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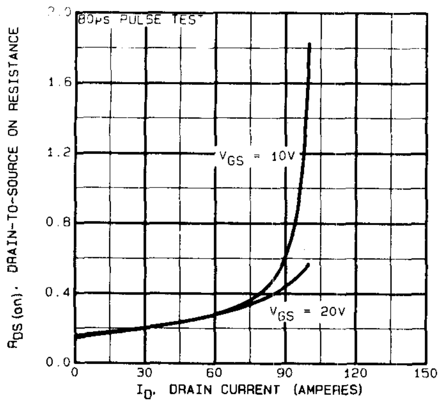

Fig. 12 - Typical on-resistance vs. drain current.

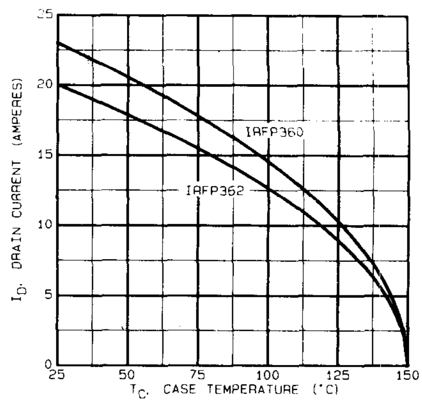

Fig. 13 - Maximum drain current vs. case temperature.

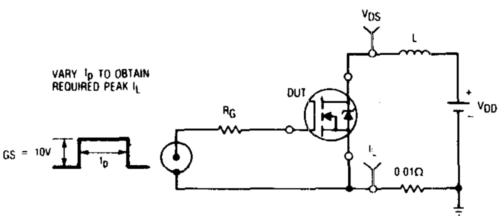

Fig. 14a - Unclamped inductive test circuit.

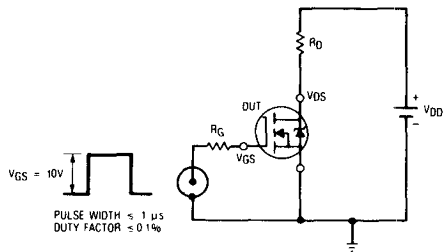

Fig. 15a - Switching time test circuit.

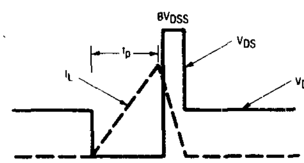

Fig. 14b - Unclamped inductive waveforms.

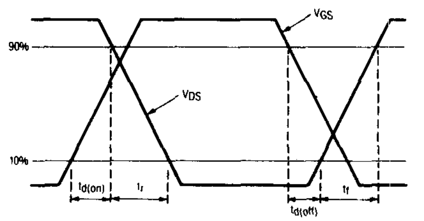

Fig. 15b - Switching time waveforms.

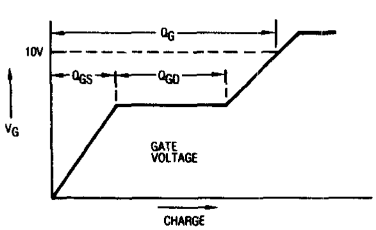

Fig. 16a - Basic gate charge waveform.

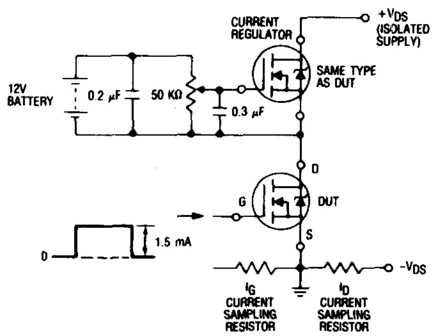

Fig. 16b - Gate charge test circuit.