TOSHIBA GTR MODULE SILICON N CHANNEL IGBT

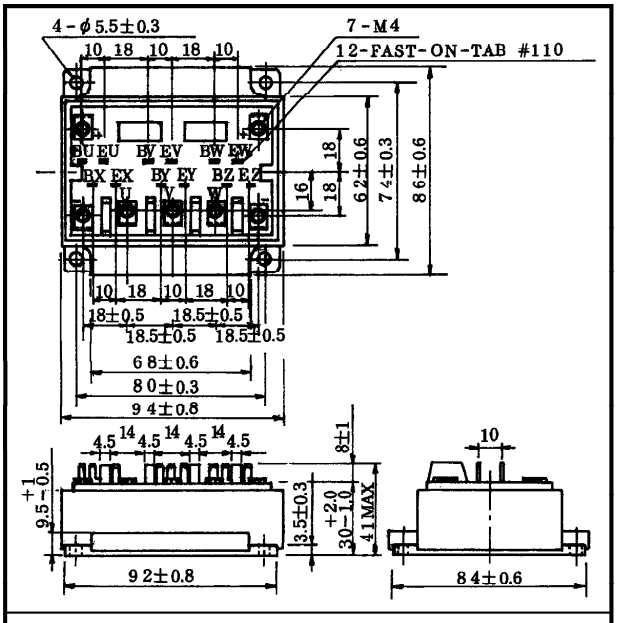
MG75J6ES50

HIGH POWER SWITCHING APPLICATIONS.

MOTOR CONTROL APPLICATIONS.

- The Electrodes are Isolated from Case.
- High Input Impedance.
- 6 IGBTs Built Into 1 Package.
- Enhancement-Mode.
- High Speed : $t_f = 0.30\mu s$ (Max.) ($I_C = 75A$)
  $t_{rr} = 0.15\mu s$ (Max.) ($I_F = 75A$)
- Low Saturation Voltage
  : $V_{CE\ (sat)} = 2.70V$ (Max.) ($I_C = 75A$)

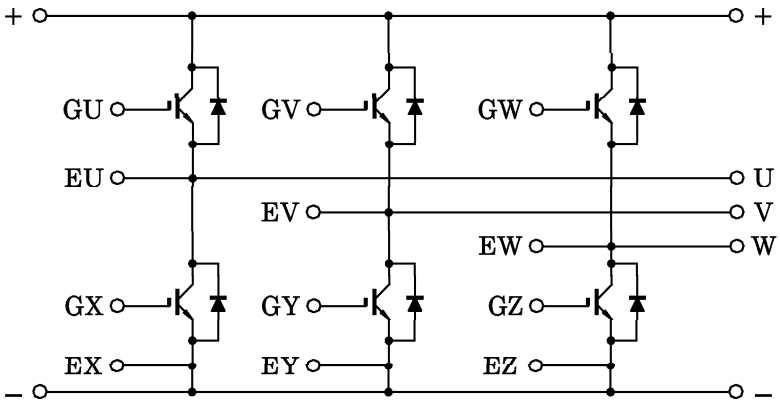
Unit in mm



JEDEC	—
EIAJ	—
TOSHIBA	2-94A2A

Weight : 505g (TYP.)

EQUIVALENT CIRCUIT



961001EAA2

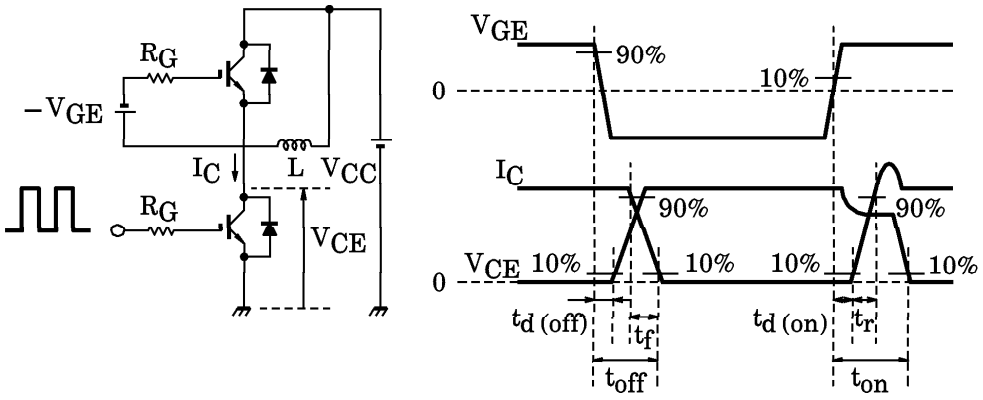
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Collector-Emitter Voltage		V_{CES}	600	V
Gate-Emitter Voltage		V_{GES}	±20	V
Collector Current	DC	I_C	75	A
	1ms	I_{CP}	150	
Forward Current	DC	I_F	75	A
	1ms	I_{FM}	150	
Collector Power Dissipation (Tc = 25°C)		P_C	390	W
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_{stg}	−40~125	°C
Isolation Voltage		V_{Isol}	2500 (AC 1 min.)	V
Screw Torque (Terminal / Mounting)		—	2 / 3	N·m

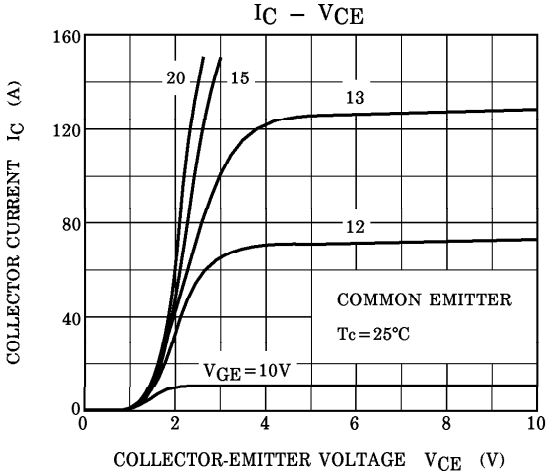
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GES}	V_{GE} = ±20V, V_{CE} = 0	—	—	±500	nA
Collector Cut-off Current		I_{CES}	V_{CE} = 600V, V_{GE} = 0	—	—	1.0	mA
Gate-Emitter Cut-off Voltage		$V_{GE\ (off)}$	I_C = 7.5mA, V_{CE} = 5V	5.0	7.0	8.0	V
Collector-Emitter Saturation Voltage		$V_{CE\ (sat)}$	I_C = 75A, V_{GE} = 15V	—	2.10	2.70	V
Input Capacitance		C_{ies}	V_{CE} = 10V, V_{GE} = 0, f = 1MHz	—	7100	—	pF
Switching Time	Turn-on Delay Time	$t_{d\ (on)}$	Inductive Load V_{CC} = 300V I_C = 75A V_{GE} = ±15V R_G = 18Ω (Note 1)	—	0.08	0.16	μs
	Rise Time	t_r		—	0.12	0.24	
	Turn-on Time	t_{on}		—	0.40	0.80	
	Turn-off Delay Time	$t_{d\ (off)}$		—	0.20	0.40	
	Fall Time	t_f		—	0.15	0.30	
	Turn-off Time	t_{off}		—	0.50	1.00	
Forward Voltage		V_F	I_F = 75A, V_{GE} = 0	—	2.10	2.80	V
Reverse Recovery Time		t_{rr}	I_F = 75A, V_{GE} = −10V di / dt = 100A / μs	—	0.08	0.15	μs
Thermal Resistance		$R_{th\ (j-c)}$	Transistor	—	—	0.32	°C / W
			Diode	—	—	0.69	

Note 1 Switching Time Test Circuit & Timing Chart



I_C – V_{CE}



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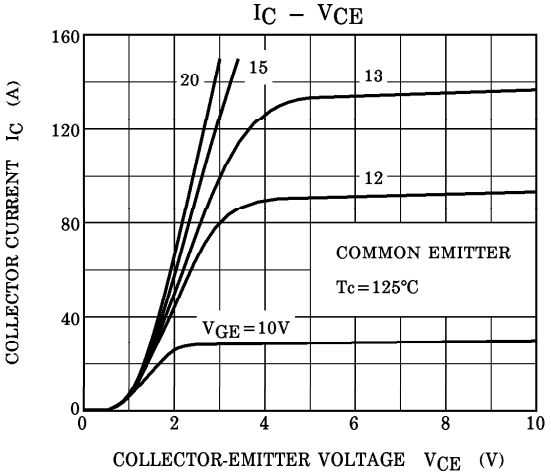
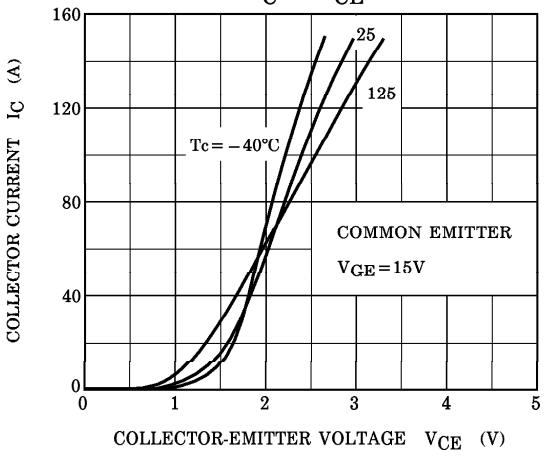
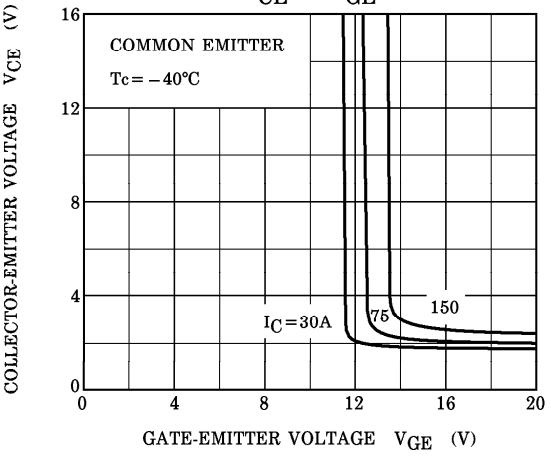


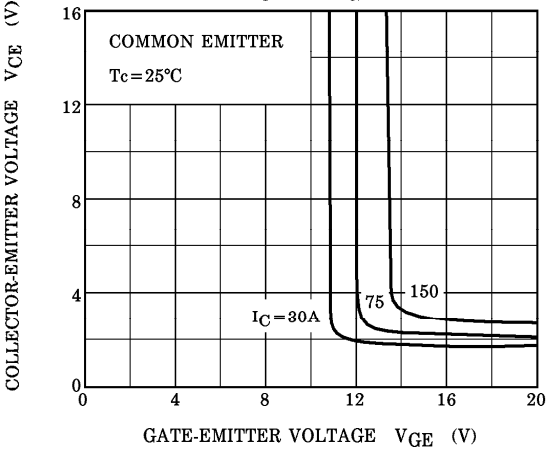
I_C – V_{CE}



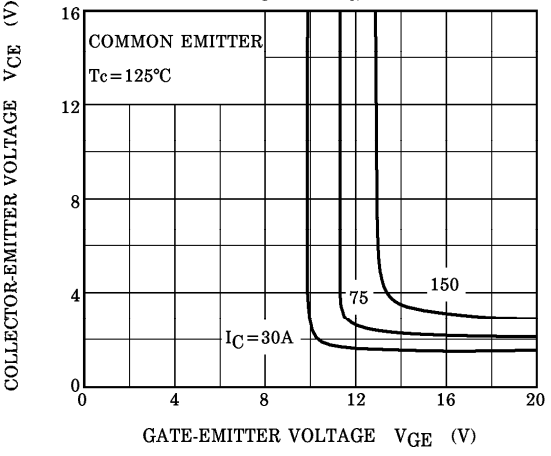
V_{CE} – V_{GE}



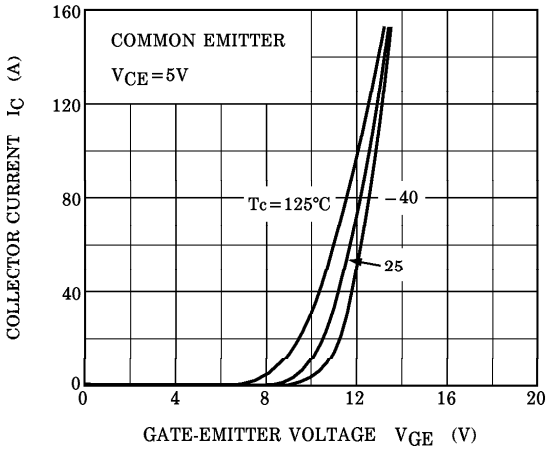
V_{CE} – V_{GE}



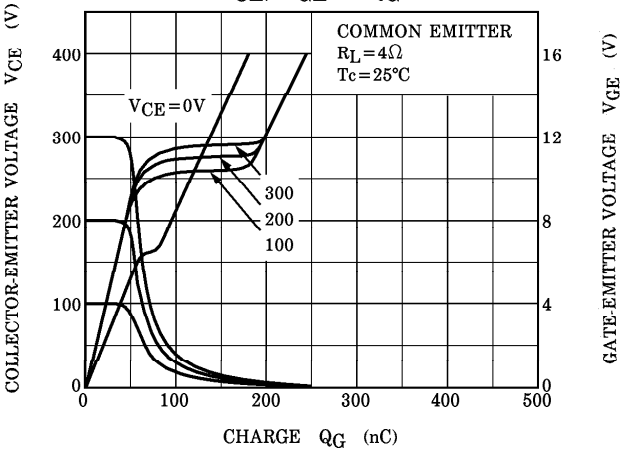
V_{CE} – V_{GE}



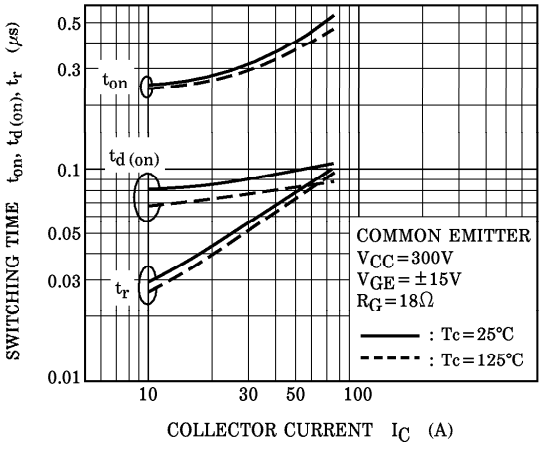
I_C – V_{GE}



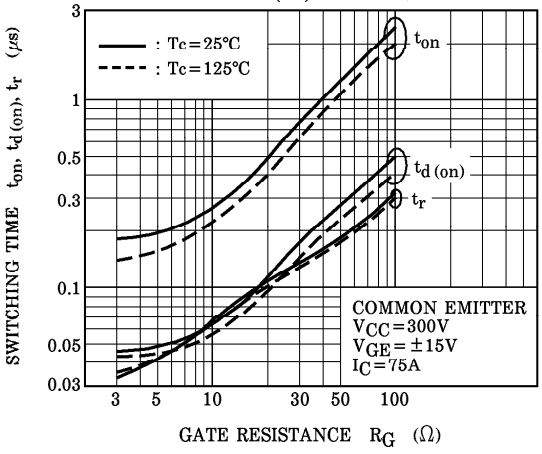
V_{CE}, V_{GE} – Q_G



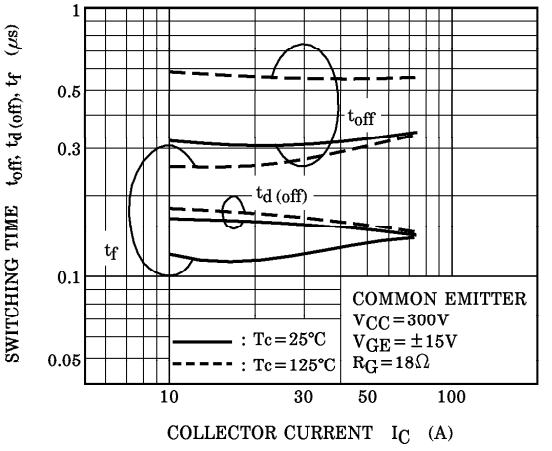
t_{on}, $t_{d\,(on)}$, t_r – I_C



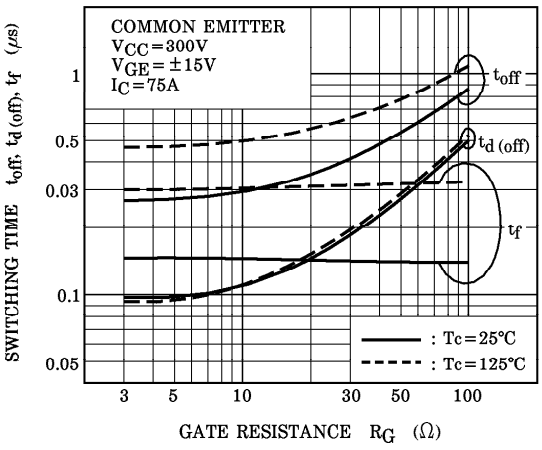
t_{on}, $t_{d\,(on)}$, t_r – R_G



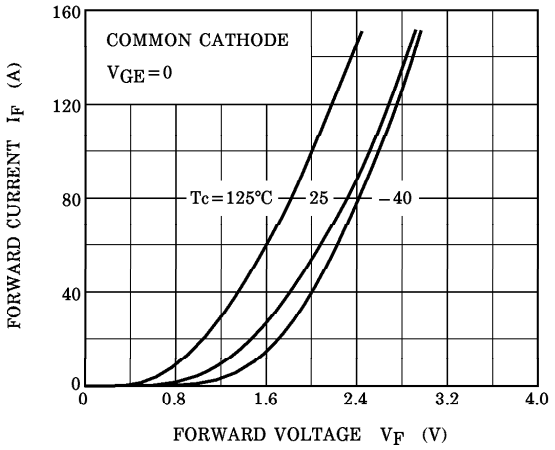
t_{off}, $t_{d\,(off)}$, t_f – I_C



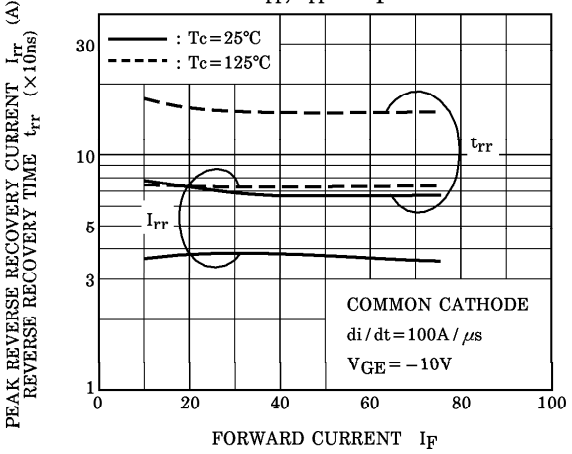
t_{off}, $t_{d\,(off)}$, t_f – R_G



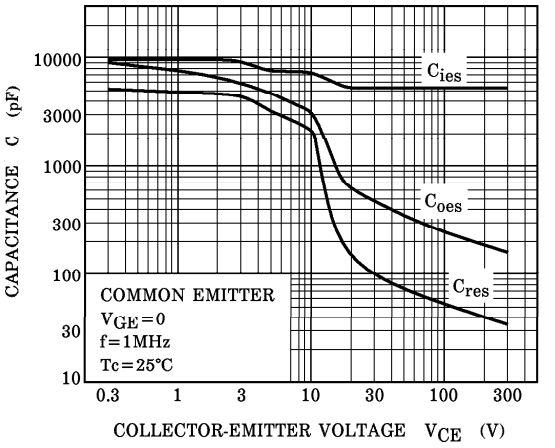
$I_F - V_F$



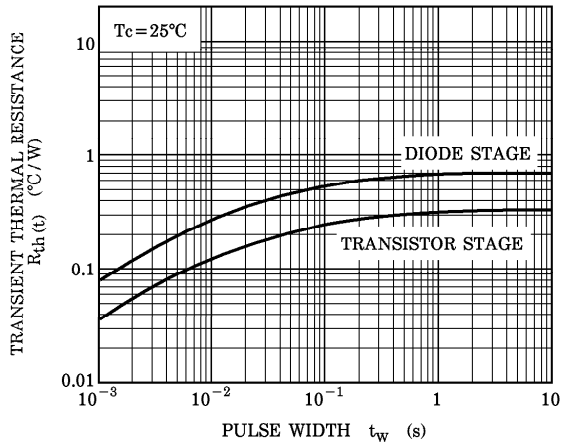
$t_{rr}, I_{rr} - I_F$



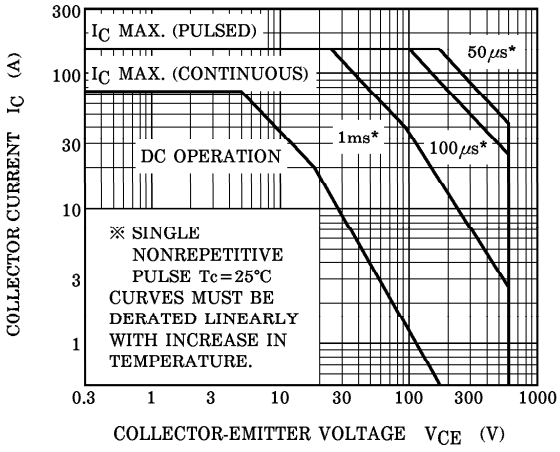
$C - V_{CE}$



$R_{th\,(t)} - t_w$



SAFE OPERATING AREA



REVERSE BIAS SOA