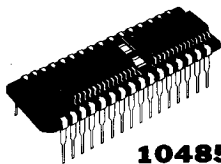


MH12808TNA-85,-10,-12,-15

1048576-BIT(131072-WORD BY 8-BIT) CMOS STATIC RAM MODULE


DESCRIPTION

The MH12808TNA is a 1048576-bits CMOS static RAM module organized as 131072-words by 8-bits. It consists of four industry standard 32K x 8 static RAMs and one decoder.

The stand-by current is low enough for a battery backup application. It is mounted a flat package on a 32-pin dual in line package and configured in an industrial standard 128K x 8-bits pin out.

FEATURES

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
MH12808TNA-85	85ns	70 mA	200 μ A
MH12808TNA-10	100ns		
MH12808TNA-12	120ns		
MH12808TNA-15	150ns		

- JEDEC standard 32-pin 600mil pin out
- Single +5V Power Supply
- No Clocks, No Refresh
- Data-Hold on +2V Power Supply
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expansion by $\bar{S}$
- OE Prevents Data Contention in the I/O Bus
- Common Data I/O

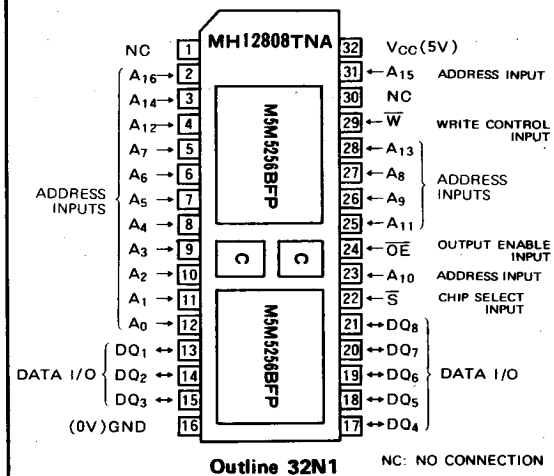
APPLICATION

Small Capacity Memory Units.

FUNCTION

The operation mode of the MH12808TNA is determined by a combination of the device control inputs $\bar{S}$, $\bar{W}$ and $\bar{OE}$. Each mode is summarized in the function table. (see next page)

PIN CONFIGURATION (TOP VIEW)

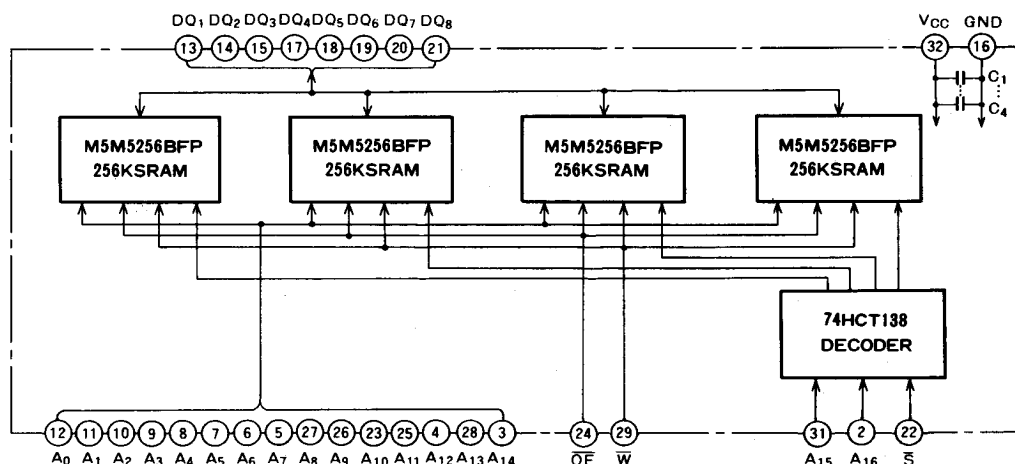


A write cycle is executed whenever the low level $\bar{W}$ overlaps with the low level $\bar{S}$. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\bar{W}$, $\bar{S}$, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable $\bar{OE}$ directly controls the output stage. Setting the $\bar{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\bar{W}$ at a high level and $\bar{OE}$ at a low level while $\bar{S}$ are in an active state.

When setting $\bar{S}$ at a high level, the chip is in a non-

BLOCK DIAGRAM



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selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\bar{S}$. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4} , and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\bar{S}$	$\bar{W}$	$\bar{OE}$	Mode	DQ	I_{CC}
H	X	X	Non selection	High-impedance	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		High-impedance	Active

RECOMMENDED OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	Low input voltage	-0.3		0.8	V
V_{IH}	High input voltage	2.2		$V_{CC}+0.3$	V

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	-0.3 ~ 7	V
V_I	Input voltage		-0.3 ~ $V_{CC} + 0.3$	V
V_O	Output voltage		0 ~ V_{CC}	V
P_d	Power dissipation	$T_a = 25^\circ\text{C}$	700	mW
T_{opr}	Operating temperature		0 ~ 70	$^\circ\text{C}$
T_{stg}	Storage temperature		-40 ~ 125	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High input voltage		2.2		$V_{CC}+0.3$	V
V_{IL}	Low input voltage		-0.3		0.8	V
V_{OH}	High output voltage	$I_{OH} = -1\text{mA}$	2.4			V
V_{OL}	Low output voltage	$I_{OL} = 2\text{mA}$			0.4	V
I_I	Input current	$V_I = 0 \sim V_{CC}$			± 1	μA
I_{OZH}	High level output current in off-state	$\bar{S} = V_{IH}$ or $\bar{OE} = V_{IH}$			1	μA
I_{OZL}	Low level output current in off-state	$V_{I/O} = 0 \sim V_{CC}$			-1	μA
I_{CC1}	Active supply current (AC. MOS level)	$\bar{S} < 0.2$, $\bar{W} > V_{CC} - 0.3$ output open other input < 0.2 or $> V_{CC} - 0.3$ Min. cycle		30	65	mA
I_{CC2}	Active supply current (AC. TTL level)	$\bar{S} = V_{IL}$, $\bar{W} = V_{IH}$ output open other input $= V_{IL}$ or V_{IH} Min. cycle		35	70	mA
I_{CC3}	Stand-by supply current	$\bar{S} \approx V_{CC} - 0.2\text{V}$ A_{15} and $A_{16} \approx 0.2$ or $\approx V_{CC} - 0.2$ Other inputs $= 0 \sim V_{CC}$			200	μA
I_{CC4}	Stand-by supply current	$\bar{S} = V_{IH}$, Other inputs $= 0 \sim V_{CC}$			3	mA
C_i	Input capacitance ($T_a = 25^\circ\text{C}$)	$V_I = \text{GND}$, $V_i = 25\text{mVrms}$, $f = 1\text{MHz}$			30	pF
C_o	Output capacitance ($T_a = 25^\circ\text{C}$)	$V_O = \text{GND}$, $V_O = 25\text{mVrms}$, $f = 1\text{MHz}$			30	pF

Note 1: Direction for current flowing into IC is indicated as positive (no mark)

2: Typical value is $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$

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SWITCHING CHARACTERISTICS (Ta=0~70°C, VCC=5V±10%, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits												Unit
		MH12808TNA-85			MH12808TNA-10			MH12808TNA-12			MH12808TNA-15			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{CR}	Read cycle time	85			100			120			150			ns
t _a (A)	Address access time			85			100			120			150	ns
t _a (S)	Chip select access time			85			100			120			150	ns
t _a (OE)	Output enable access time			45			50			60			75	ns
t _{dis} (S)	Output disable time after $\overline{S}$ high			30			35			40			45	ns
t _{dis} (OE)	Output disable time after $\overline{OE}$ high			30			35			40			45	ns
t _{en} (S)	Output enable time after $\overline{S}$ low	10			10			10			10			ns
t _{en} (OE)	Output enable time after $\overline{OE}$ low	10			10			10			10			ns
t _v (A)	Data valid time after address change	20			20			20			20			ns

TIMING REQUIREMENTS (Ta=0~70°C, VCC=5V±10%, unless otherwise noted)

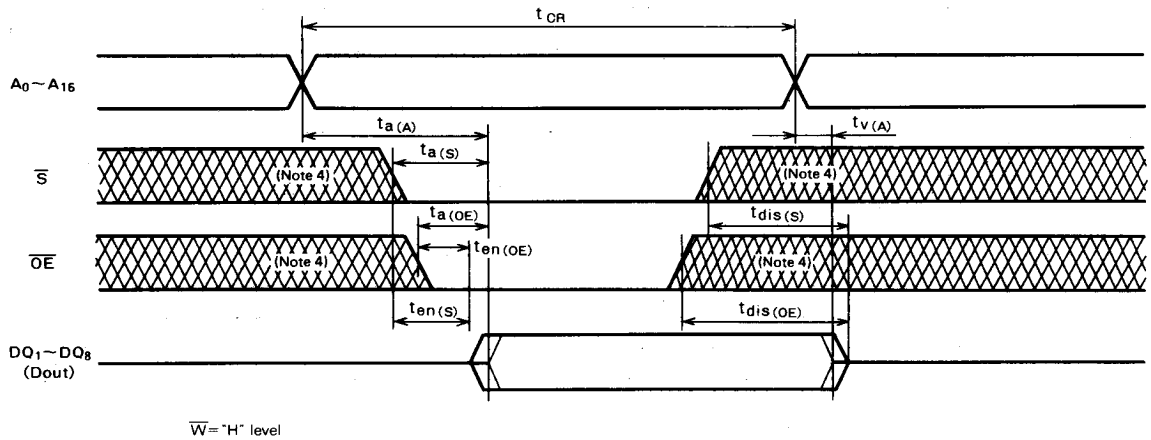
Write cycle

Symbol	Parameter	Limits												Unit
		MH12808TNA-85			MH12808TNA-10			MH12808TNA-12			MH12808TNA-15			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t _{OW}	Write cycle time	85			100			120			150			ns
t _{W(W)}	Write pulse width	60			60			70			80			ns
t _{SU(A)}	Address set up time	0			0			0			0			ns
t _{SU(A-$\overline{WH}$)}	Address set up time with respect to $\overline{W}$ high	75			80			85			90			ns
t _{SU(S)}	Chip select set up time	75			80			85			90			ns
t _{SU(D)}	Data set up time	35			35			40			50			ns
t _{H(D)}	Data hold time	0			0			0			0			ns
t _{rec(W)}	Write recovery time	0			0			0			0			ns
t _{dis(W)}	Output disable time after $\overline{W}$ low			30			35			40			45	ns
t _{dis(OE)}	Output disable time after $\overline{OE}$ high			30			35			40			45	ns
t _{en(W)}	Output enable time after $\overline{W}$ high	10			10			10			10			ns
t _{en(OE)}	Output enable time after $\overline{OE}$ low	10			10			10			10			ns

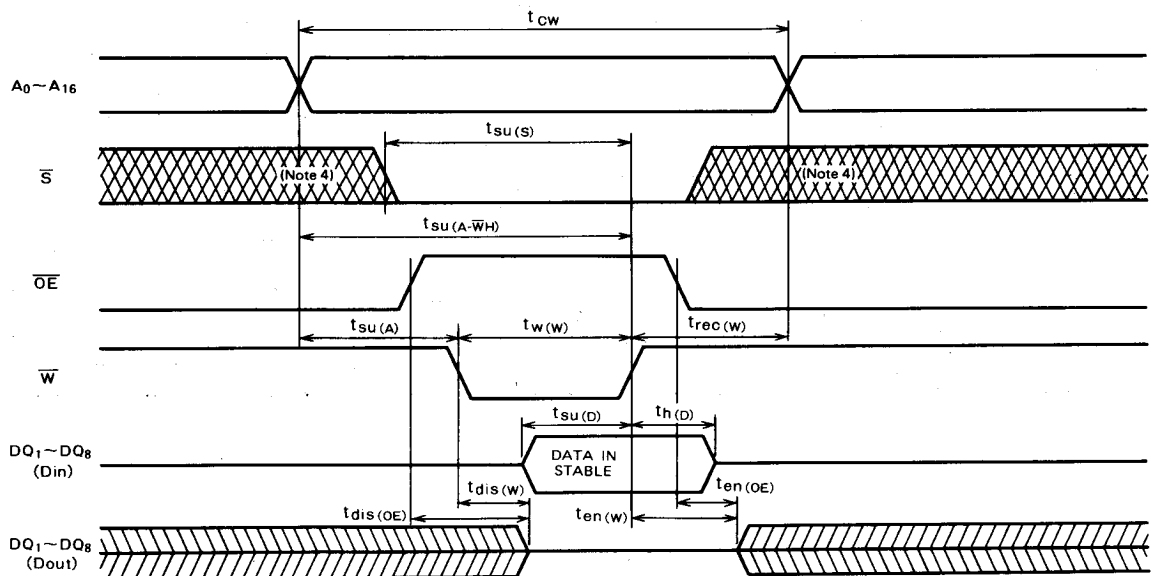
1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM MODULE

TIMING DIAGRAM

Read cycle



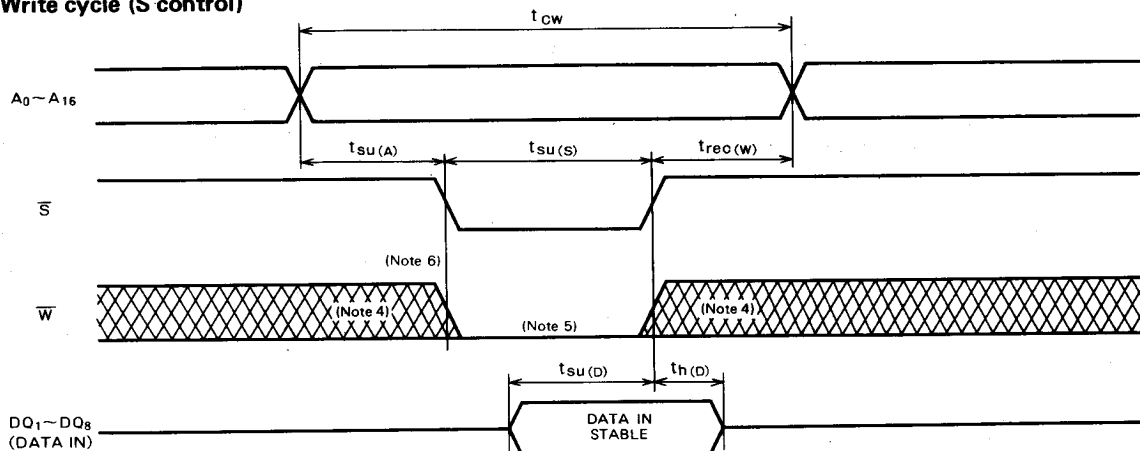
Write cycle ($\overline{W}$ control)



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Write cycle ($\bar{S}$ control)



Note 3: Test condition

Input pulse level: 0.6 ~ 2.4V

Input pulse rise fall time: 10ns

Load: 1 TTL, $C_L = 100\text{pF}$

Conditions of assessment: 1.5V

4: Hatching indicates the state is don't care.

5: Writing is executed in overlap of $\bar{S}$ and $\bar{W}$ low.

6: If $\bar{W}$ goes low simultaneously with or prior to $\bar{S}$, the output remains in the high-impedance state.

7: Don't active inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2			V
$V_I(\bar{S})$	Chip select input $\bar{S}$	$2.2\text{V} \leq V_{CC(PD)}$	2.2			V
		$2\text{V} \leq V_{CC(PD)} \leq 2.2\text{V}$		$V_{CC(PD)}$		V
$I_{CC(PD)}$	Power down supply current	$V_{CC} = 3\text{V}$, A_{15} and $A_{16} < 0.2$ or $> V_{CC} - 0.2$, Other inputs $= 0 \sim V_{CC}$			100	μA

TIMING REQUIREMENTS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PD)}$	Power down setup time		0			ns
$t_{rec(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS

