TOSHIBA GTR MODULE SILICON N CHANNEL IGBT

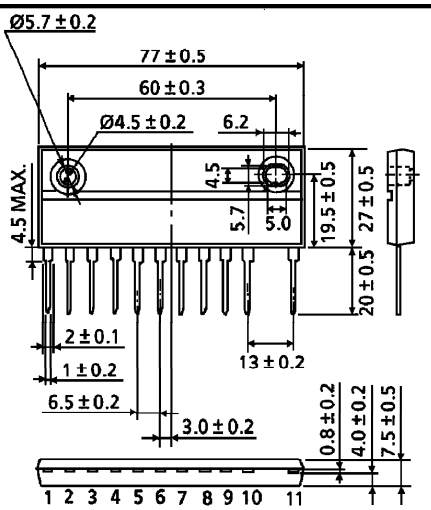
MP6759

MOTOR CONTROL APPLICATIONS

HIGH POWER SWITCHING APPLICATIONS

- The Electrodes are Isolated from Case.
- 6 IGBTs are Built Into 1 Package.
- Enhancement-Mode
- Low Saturation Voltage
  : $V_{CE\ (sat)}$ = 2.7 V (Max.) (I_C = 10 A)
- High Speed
  : t_f = 0.35 μs (Max.) (I_C = 10 A)

Unit in mm

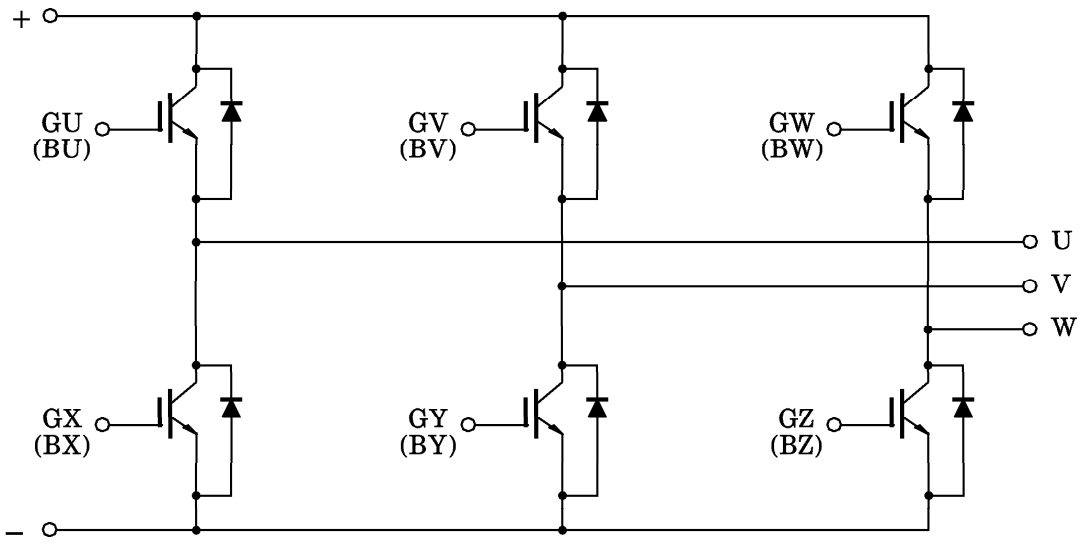


1. (+) 2. GU 3. U 4. GV 5. V 6. GW
7. W 8. GX 9. GY 10. GZ 11. (−)

JEDEC	—
EIAJ	—
TOSHIBA	2-78A1A

Weight : 44 g (Typ.)

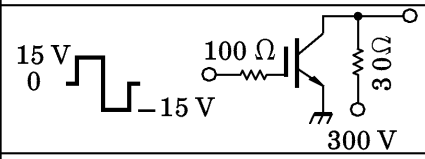
EQUIVALENT CIRCUIT



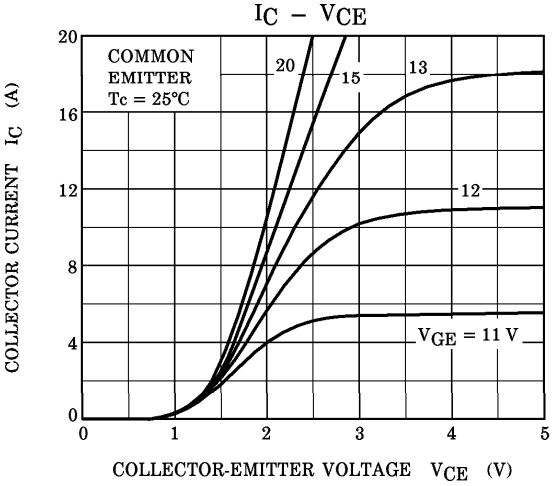
MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Collector-Emitter Voltage		V_{CES}	600	V
Gate-Emitter Voltage		V_{GES}	±20	V
Collector Current	DC	I_C	10	A
	1 ms	I_{CP}	20	
Forward Current	DC	I_F	10	A
	1 ms	I_{FM}	20	
Collector Power Dissipation (Tc = 25°C)		P_C	40	W
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_{stg}	−40~125	°C
Isolation Voltage		V_{ISOL}	2500 (AC 1 minute)	V
Screw Torque		—	1.5	N·m

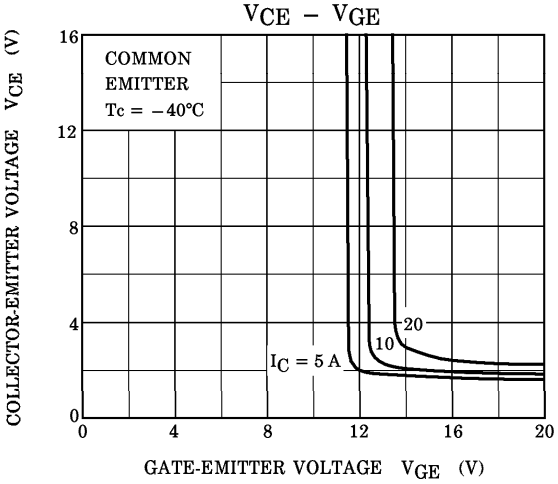
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GES}	V_{GE} = ±20 V, V_{CE} = 0	—	—	±200	nA
Collector Cut-off Current		I_{CES}	V_{CE} = 600 V, V_{GE} = 0	—	—	1	mA
Gate-Emitter Cut-off Voltage		$V_{GE\ (OFF)}$	I_C = 1 mA, V_{CE} = 5 V	5	—	8	V
Collector-Emitter Saturation Voltage		$V_{CE\ (sat)}$	I_C = 10 A, V_{GE} = 15 V	—	2.1	2.7	V
Input Capacitance		C_{ies}	V_{CE} = 10 V, V_{GE} = 0, f = 1 MHz	—	720	—	pF
Switching Time	Rise Time	t_r		—	0.3	—	μs
	Turn-on Time	t_{on}		—	0.4	—	
	Fall Time	t_f		—	0.2	0.35	
	Turn-off Time	t_{off}		—	0.4	—	
Forward Voltage		V_F	I_F = 10 A, V_{GE} = 0	—	—	2.0	V
Reverse Recovery time		t_{rr}	I_F = 10 A, di / dt = −100 A / μs	—	—	200	ns
Thermal Resistance		$R_{th\ (j\text{-}c)}$	Transistor	—	—	3.09	°C / W
			Diode	—	—	4.77	

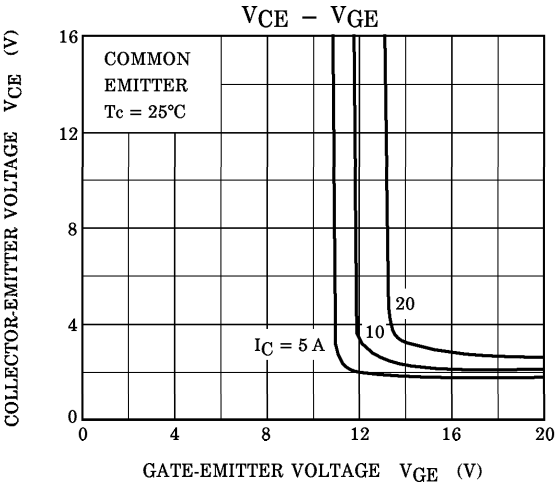
$I_C - V_{CE}$



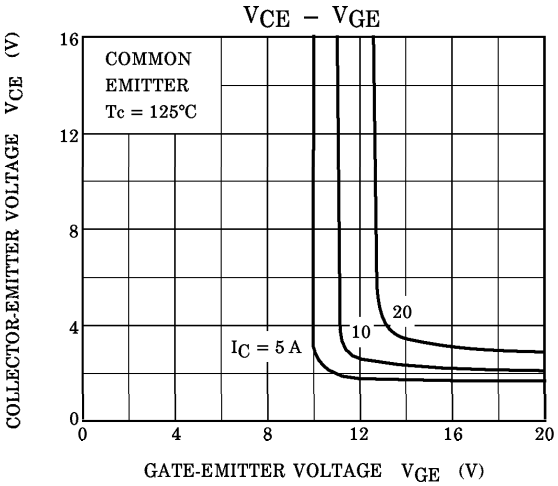
$V_{CE} - V_{GE}$



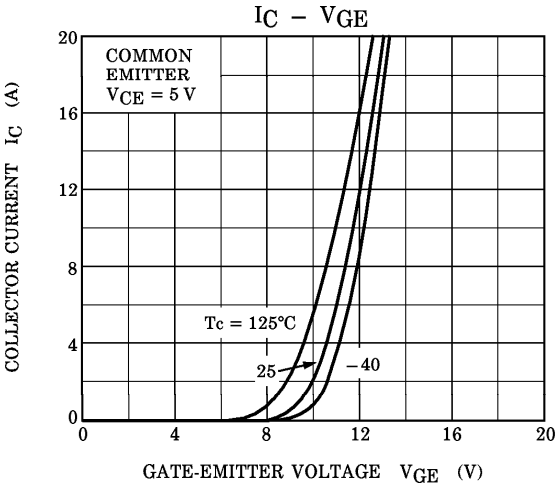
$V_{CE} - V_{GE}$



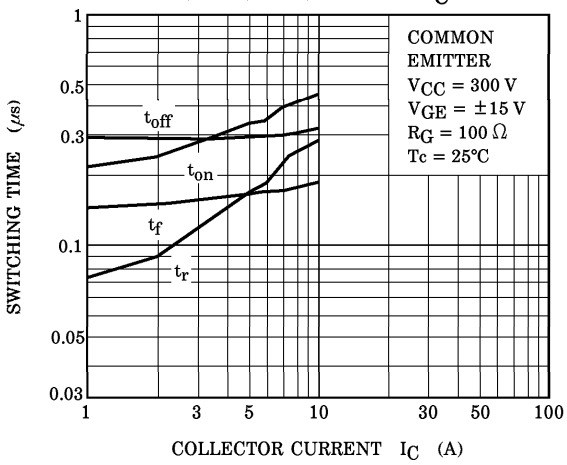
$V_{CE} - V_{GE}$



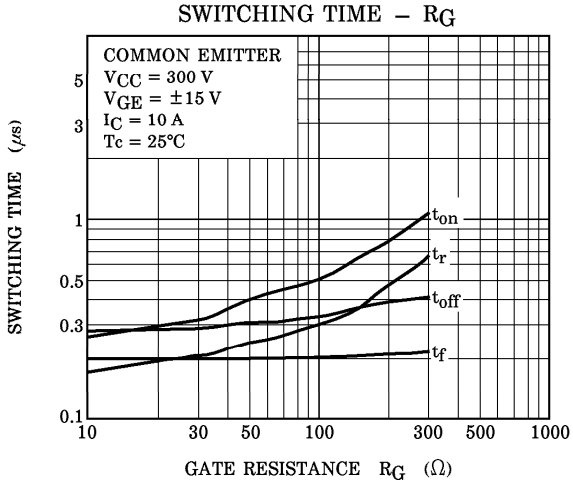
$I_C - V_{GE}$



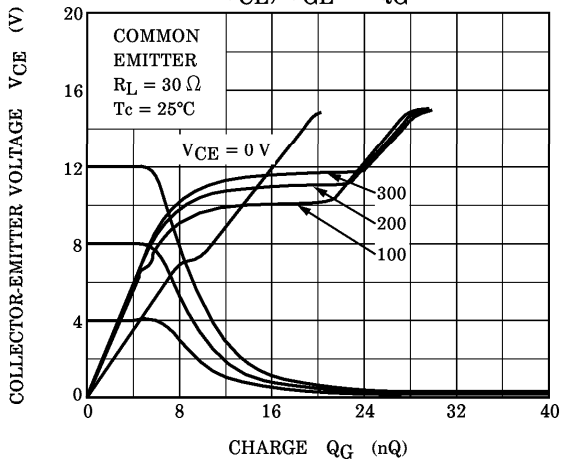
SWITCHING TIME – I_C



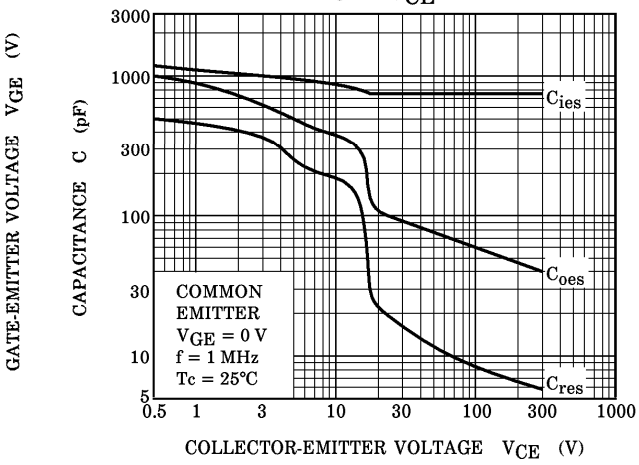
SWITCHING TIME – R_G



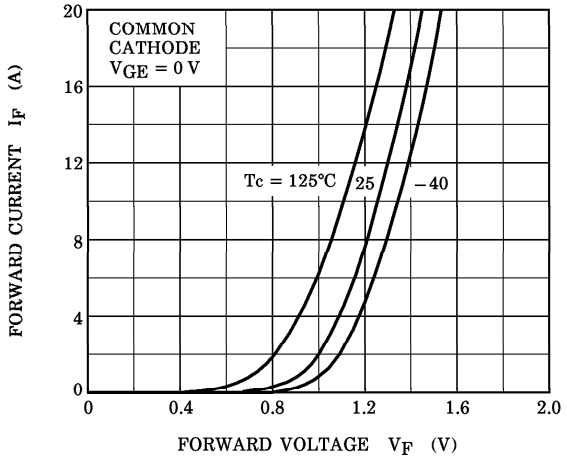
V_{CE}, V_{GE} – Q_G



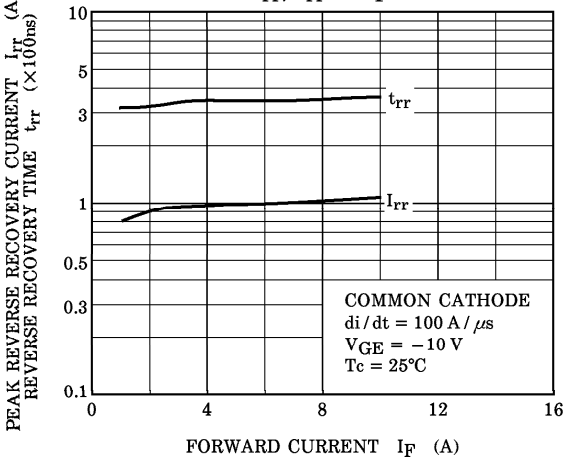
C – V_{CE}



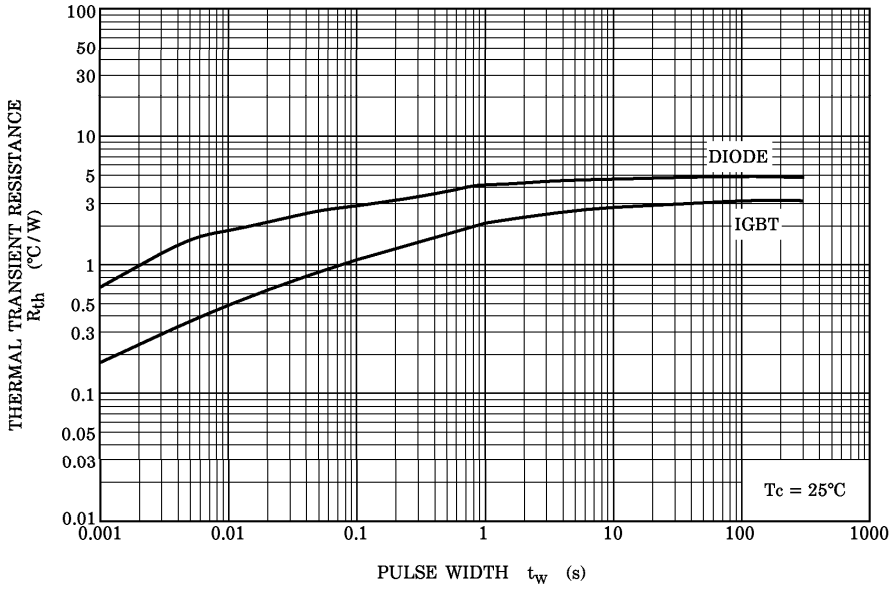
I_F – V_F



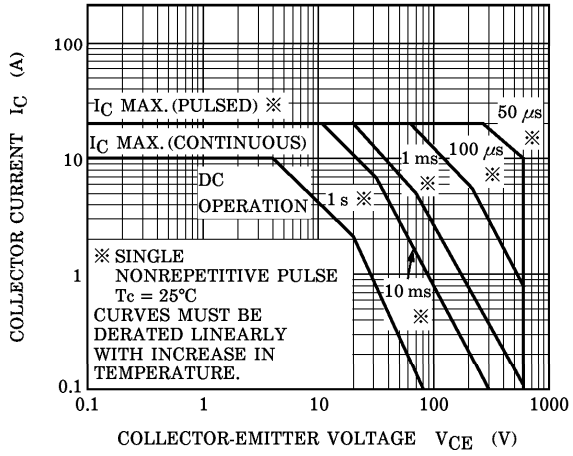
t_{rr}, I_{rr} – I_F



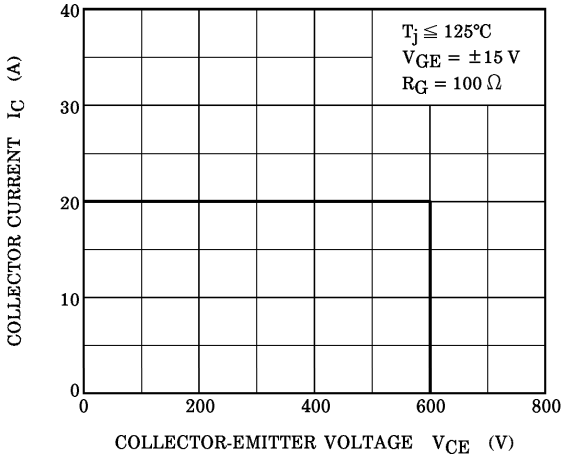
$R_{th} - t_w$



SAFE OPERATING AREA



REVERSE BIAS AREA



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