
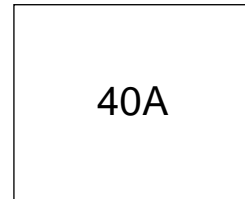


### PASSIVATED ASSEMBLED CIRCUIT ELEMENTS

#### Features

- Glass passivated junctions for greater reliability
- Electrically isolated base plate
- Available up to 1200 V<sub>RRM</sub>, V<sub>DRM</sub>
- High dynamic characteristics
- Wide choice of circuit configurations
- Simplified mechanical design and assembly
- UL E78996 approved 



#### Description

The P400 series of Integrated Power Circuits consists of power thyristors and power diodes configured in a single package. With its isolating base plate, mechanical designs are greatly simplified giving advantages of cost reduction and reduced size.

Applications include power supplies, control circuits and battery chargers.

#### Major Ratings and Characteristics

Parameters	P400	Units
I <sub>D</sub>	40	A
@ T <sub>C</sub>	80	°C
I <sub>FSM</sub>	@ 50Hz	385 A
	@ 60Hz	400 A
I <sup>2</sup> t	@ 50Hz	745 A <sup>2</sup> s
	@ 60Hz	680 A <sup>2</sup> s
I <sup>2</sup> √t	7450	A <sup>2</sup> √s
V <sub>RRM</sub>	400 to 1200	V
V <sub>INS</sub>	2500	V
T <sub>J</sub>	- 40 to 125	°C

## P400 Series

Bulletin I2776 rev. E 04/99

International  
 Rectifier

### ELECTRICAL SPECIFICATIONS

#### Voltage Ratings

Type number	$V_{RRM}$ maximum repetitive peak reverse voltage V	$V_{RSM}$ maximum non-repetitive peak reverse voltage V	$V_{DRM}$ maximum repetitive peak off-state voltage V	$I_{RRM}$ max. @ $T_J$ max. mA
P401, P421, P431	400	500	400	10
P402, P422, P432	600	700	600	
P403, P423, P433	800	900	800	
P404, P424, P434	1000	1100	1000	
P405, P425, P435	1200	1300	1200	

#### On-state Conduction

Parameter	P400	Units	Conditions	
$I_D$ Maximum DC output current	40	A	@ $T_C = 80^\circ\text{C}$ , full bridge circuits	
$I_{TSM}$ Max. peak one-cycle non-repetitive on-state or forward current	385	A	t = 10ms No voltage reappplied	
$I_{FSM}$	400		t = 8.3ms	100% $V_{RRM}$ reappplied
	325		t = 10ms	Sinusoidal half wave, Initial $T_J = T_J$ max.
	340		t = 8.3ms	
$I^2t$ Maximum $I^2t$ for fusing	745	$A^2s$	t = 10ms No voltage reappplied	
	680		t = 8.3ms	100% $V_{RRM}$ reappplied
	530		t = 10ms	Initial $T_J = T_J$ max.
	480		t = 8.3ms	
$I^2\sqrt{t}$ Maximum $I^2\sqrt{t}$ for fusing	7450	$A^2\sqrt{s}$	t = 0.1 to 10ms, no voltage reappplied $I^2t$ for time $tx = I^2\sqrt{t} \cdot \sqrt{tx}$	
$V_{T(TO)1}$ Low value of threshold voltage	0.83	V	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ , $T_J = T_J$ max.	
$V_{T(TO)2}$ High value of threshold voltage	1.03		$(I > \pi \times I_{T(AV)})$ , $T_J = T_J$ max.	
$r_{t1}$ Low level value of on-state slope resistance	9.61	m $\Omega$	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ , $T_J = T_J$ max.	
$r_{t2}$ High level value of on-state slope resistance	7.01		$(I > \pi \times I_{T(AV)})$ , $T_J = T_J$ max.	
$V_{TM}$ Max. peak on-state or forward voltage drop $V_{FM}$	1.4	V	$T_J = 25^\circ\text{C}$ , $I_{TM} = \pi \times I_{T(AV)}$ $T_J = 25^\circ\text{C}$ , $I_{TM} = \pi \times I_{F(AV)}$	
di/dt Maximum non repetitive rate of rise of turned on current	200	A/ $\mu s$	$T_J = 125^\circ\text{C}$ from 0.67 $V_{DRM}$ $I_{TM} = \pi \times I_{T(AV)}$ , $I_g = 500\text{mA}$ , $tr < 0.5\mu s$ , $tp > 6\mu s$	
$I_H$ Maximum holding current	130	mA	$T_J = 25^\circ\text{C}$ anode supply = 6V, resistive load	
$I_L$ Maximum latching current	250	mA	$T_J = 25^\circ\text{C}$ anode supply = 6V, resistive load	

**Blocking**

Parameter	P400	Units	Conditions
dv/dt Maximum critical rate of rise of off-state voltage	200	V/ $\mu$ s	$T_J = 125^\circ\text{C}$ , exponential to $0.67 V_{\text{DRM}}$ gate open
$I_{\text{RRM}}$ Max. peak reverse and off-state leakage current at $V_{\text{RRM}}, V_{\text{DRM}}$	10	mA	$T_J = 125^\circ\text{C}$ , gate open circuit
$I_{\text{RRM}}$ Max peak reverse leakage current	100	$\mu$ A	$T_J = 25^\circ\text{C}$
$V_{\text{INS}}$ RMS isolation voltage	2500	V	50Hz, circuit to base, all terminal shorted, $T_J = 25^\circ\text{C}$ , $t = 1\text{s}$

**Triggering**

Parameter	P400	Units	Conditions
$P_{\text{GM}}$ Maximum peak gate power	8	W	
$P_{\text{G(AV)}}$ Maximum average gate power	2		
$I_{\text{GM}}$ Maximum peak gate current	2	A	
$-V_{\text{GM}}$ Maximum peak negative gate voltage	10	V	$T_J = -40^\circ\text{C}$ $T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$ Anode Supply = 6V resistive load
$V_{\text{GT}}$ Maximum gate voltage required to trigger	3 2 1		
$I_{\text{GD}}$ Maximum gate current required to trigger	90 60 35		
$V_{\text{GD}}$ Maximum gate voltage that will not trigger	0.2	V	$T_J = 125^\circ\text{C}$ , rated $V_{\text{DRM}}$ applied
$I_{\text{GD}}$ Maximum gate current that will not trigger	2	mA	$T_J = 125^\circ\text{C}$ , rated $V_{\text{DRM}}$ applied

**Thermal and Mechanical Specification**

Parameter	P400	Units	Conditions
$T_J$ Max. operating temperature range	-40 to 125	$^\circ\text{C}$	
$T_{\text{stg}}$ Max. storage temperature range	-40 to 125		
$R_{\text{thJC}}$ Max. thermal resistance, junction to case	1.05	K/W	DC operation per junction
$R_{\text{thCS}}$ Max. thermal resistance, case to heatsink	0.10	K/W	Mounting surface, smooth and greased
T Mounting torque, base to heatsink	4	Nm	A mounting compound is recommended and the torque should be checked after a period of 3 hours to allow for the spread of the compound
wt Approximate weight	58 (2.0)	g (oz)	

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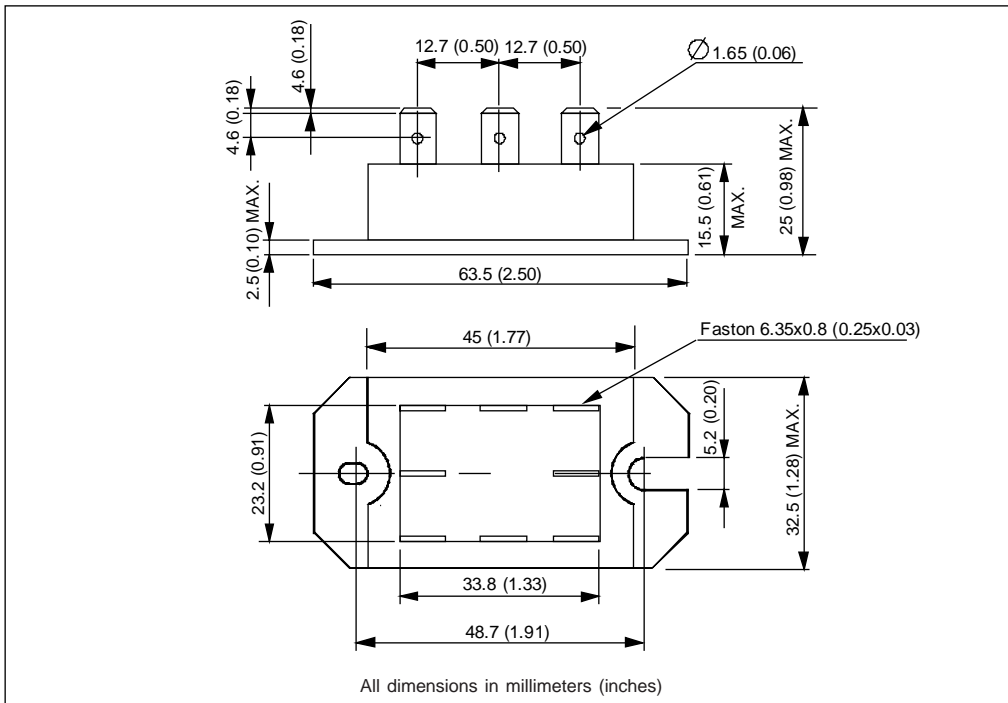
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### Circuit Type and Coding \*

	Circuit"0"	Circuit"2"	Circuit"3"
Terminal Positions			
Schematic diagram			
	SinglePhase Hybrid Bridge Common Cathode	SinglePhase Hybrid Bridge Doubler	SinglePhase AllSCR Bridge
Basic series	P40.	P42.	P43.
With voltage suppression	P40.K	P42.K	P43.K
With free-wheeling diode	P40.W	-	-
With both voltage suppression and free-wheeling diode	P40.KW	-	-

\* To complete code refer to voltage ratings table, i.e.: for 600V P410.W complete code is P402W

### Outline Table



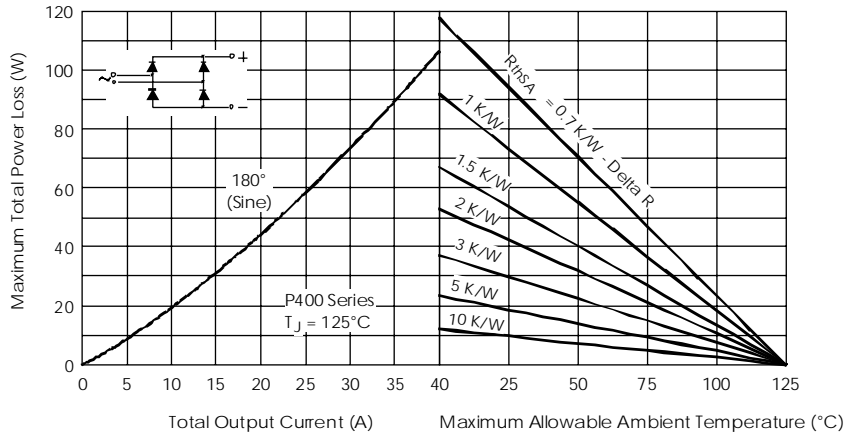


Fig. 1 - Current Ratings Nomogram (1 Module Per Heatsink)

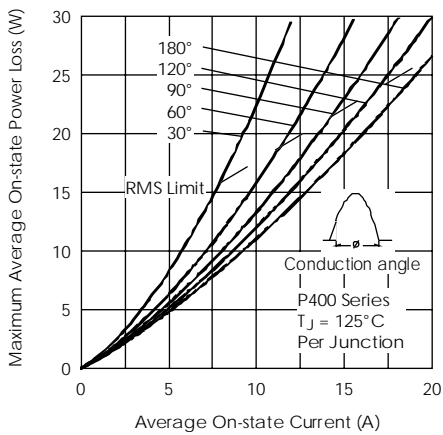


Fig. 2 - On-state Power Loss Characteristics

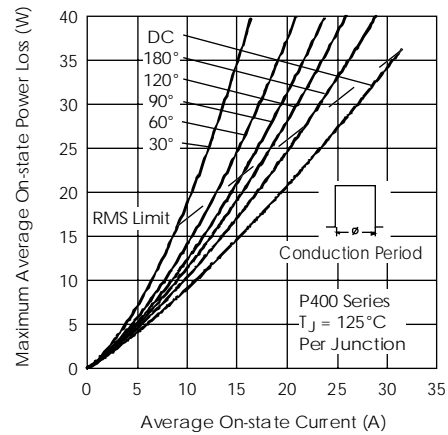


Fig. 3 - On-state Power Loss Characteristics

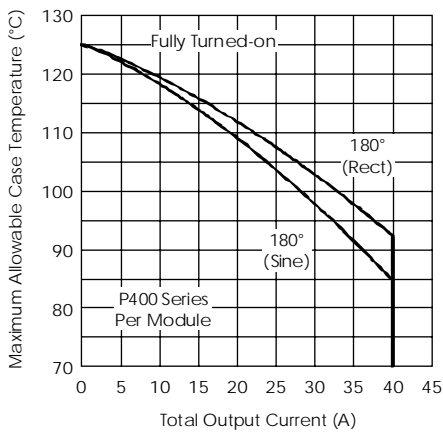


Fig. 4 - Current Ratings Characteristics

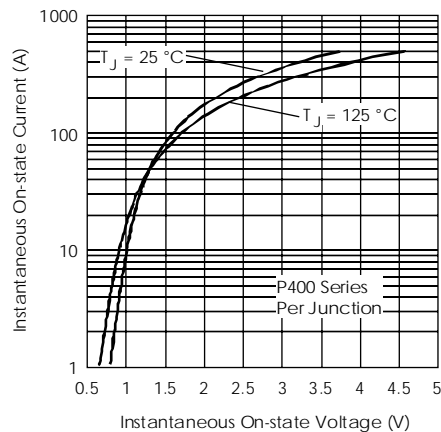


Fig. 5 - On-state Voltage Drop Characteristics

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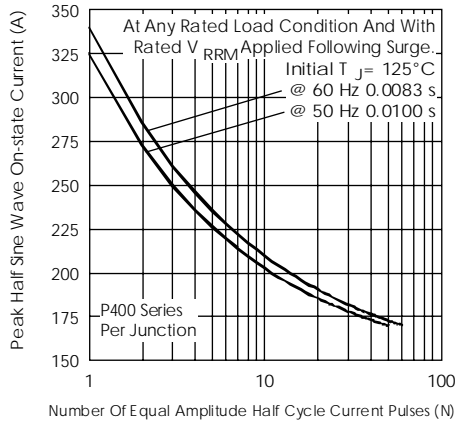


Fig. 6 - Maximum Non-Repetitive Surge Current

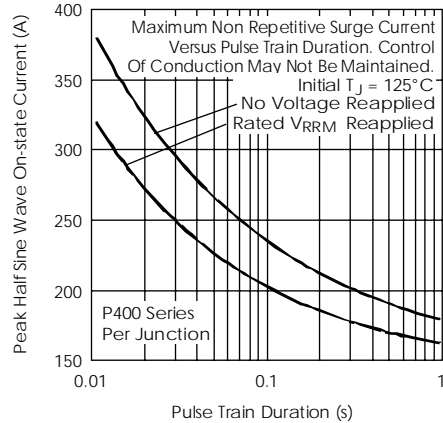


Fig. 7 - Maximum Non-Repetitive Surge Current

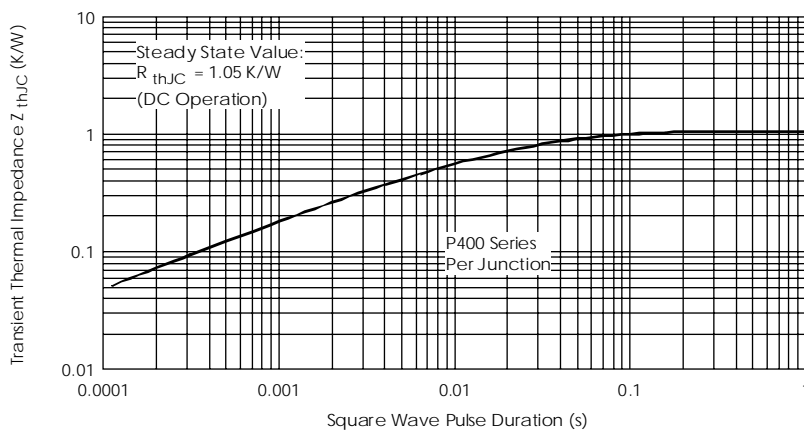


Fig. 8 - Thermal Impedance  $Z_{thJC}$  Characteristics

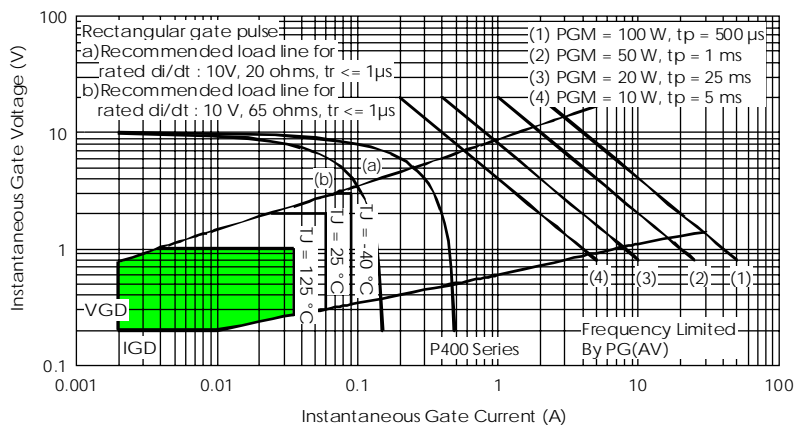


Fig. 9 - Gate Characteristics

**WORLDHEADQUARTERS:** 233 Kansas St., El Segundo, California 90245 U.S.A. Tel: (310) 322 3331. Fax: (310) 322 3332.  
**EUROPEANHEADQUARTERS:** Hurst Green, Oxted, Surrey RH8 9BB, U.K. Tel: ++ 44 1883 732020. Fax: ++ 44 1883 733408.  
**IR CANADA:** 15 Lincoln Court, Brampton, Markham, Ontario L6T3Z2. Tel: (905) 453 2200. Fax: (905) 475 8801.  
**IR GERMANY:** Saalburgstrasse 157, 61350 Bad Homburg. Tel: ++ 49 6172 96590. Fax: ++ 49 6172 965933.  
**IR ITALY:** Via Liguria 49, 10071 Borgaro, Torino. Tel: ++ 39 11 4510111. Fax: ++ 39 11 4510220.  
**IR FAR EAST:** K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo, Japan 171. Tel: 81 3 3983 0086.  
**IR SOUTHEAST ASIA:** 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994. Tel: ++ 65 838 4630.  
**IR TAIWAN:** 16 Fl. Suite D.207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan. Tel: 886 2 2377 9936.

<http://www.irf.com>

Fax-On-Demand: +44 1883 733420

Data and specifications subject to change without notice.