

PM100CSD120

FLAT-BASE TYPE
INSULATED PACKAGE

PM100CSD120



FEATURE

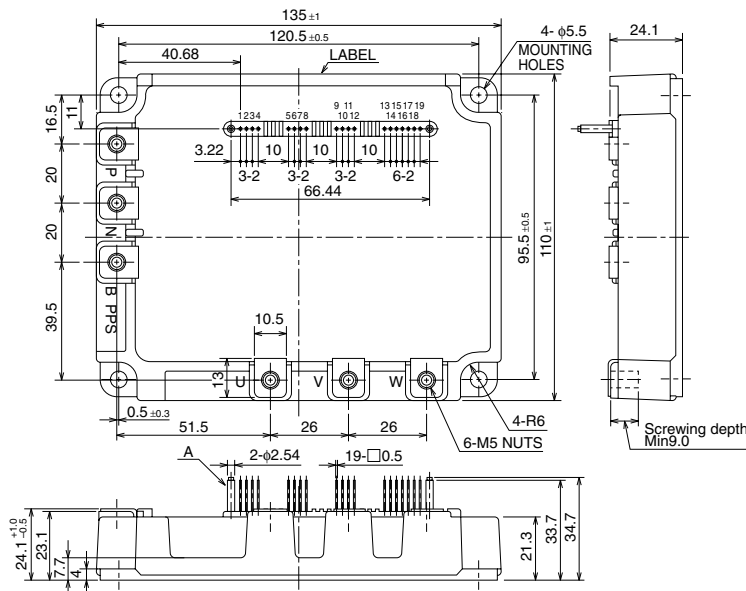
- a) Adopting new 4th generation planar IGBT chip, which performance is improved by 1μm fine rule process.
- b) Using new Diode which is designed to get soft reverse recovery characteristics.
- c) Keeping the package compatibility.
The layout/position of both terminal pin and mounting hole is same as S-series 3rd generation IPM .
- 3φ 100A, 1200V Current-sense IGBT for 15kHz switching
- Monolithic gate drive & protection logic
- Detection, protection & status indication circuits for over-current, short-circuit, over-temperature & under-voltage (P-Fo available from upper leg devices)
- Acoustic noise-less 18.5/22kW class inverter application

APPLICATION

General purpose inverter, servo drives and other motor controls

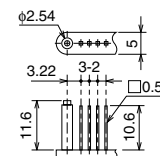
PACKAGE OUTLINES

Dimensions in mm



Terminal code

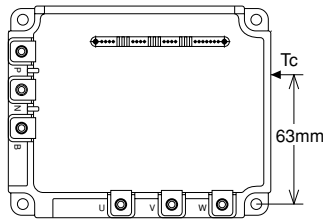
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|---------|----------|
| 1. VUPC | 11. WP |
| 2. UFO | 12. VWP1 |
| 3. UP | 13. VNC |
| 4. VUP1 | 14. VN1 |
| 5. VVPC | 15. NC |
| 6. VFO | 16. UN |
| 7. VP | 17. VN |
| 8. VVP1 | 18. WN |
| 9. VWPC | 19. Fo |
| 10. WFO | |



A : DETAIL

PM100CSD120**FLAT-BASE TYPE
INSULATED PACKAGE****TOTAL SYSTEM**

Symbol	Parameter	Condition	Ratings	Unit
V _{CC(Prot)}	Supply Voltage Protected by OC & SC	V _D = 13.5 ~ 16.5V, Inverter Part, T _j = 125°C Start	800	V
V _{CC(surge)}	Supply Voltage (Surge)	Applied between : P-N, Surge value or without switching	1000	V
T _c	Module Case Operating Temperature	(Note-1)	-20 ~ +100	°C
T _{stg}	Storage Temperature		-40 ~ +125	°C
V _{iso}	Isolation Voltage	60Hz, Sinusoidal, Charged part to Base, AC 1 min.	2500	V _{rms}

(Note-1) T_c measurement point is as shown below. (Base plate depth 3mm)**THERMAL RESISTANCES**

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-c)Q}	Junction to case Thermal Resistances	Inverter IGBT part (per 1 element), (Note-1)	—	—	0.21	°C/W
R _{th(j-c)F}		Inverter FWDi part (per 1 element), (Note-1)	—	—	0.35	
R _{th(j-c')Q}		Inverter IGBT part (per 1 element), (Note-2)	—	—	0.13	
R _{th(j-c')F}		Inverter FWDi part (per 1 element), (Note-2)	—	—	0.21	
R _{th(c-f)}	Contact Thermal Resistance	Case to fin, Thermal grease applied (per 1 module)	—	—	0.018	

(Note-2) T_c measurement point is just under the chips.If you use this value, R_{th(f-a)} should be measured just under the chips.**ELECTRICAL CHARACTERISTICS** (T_j = 25°C, unless otherwise noted)**INVERTER PART**

Symbol	Parameter	Test Condition		Limits			Unit
				Min.	Typ.	Max.	
V _{CE(sat)}	Collector-Emitter Saturation Voltage	V _D = 15V, I _C = 100A V _{CIN} = 0V, Pulsed (Fig. 1)	T _j = 25°C	—	2.4	3.2	V
			T _j = 125°C	—	2.1	2.8	
V _{EC}	FWDi Forward Voltage	-I _C = 100A, V _D = 15V, V _{CIN} = 15V (Fig. 2)		—	2.5	3.5	V
t _{on}	Switching Time	V _D = 15V, V _{CIN} = 15V↔0V V _{CC} = 600V, I _C = 100A T _j = 125°C Inductive Load (upper and lower arm) (Fig. 3)		0.5	1.0	2.5	μs
t _{rr}				—	0.15	0.3	
t _{c(on)}				—	0.4	1.0	
t _{off}				—	2.5	3.5	
t _{c(off)}				—	0.7	1.2	
I _{CES}	Collector-Emitter Cutoff Current	V _{CE} = V _{CES} , V _{CIN} = 15V (Fig. 4)	T _j = 25°C	—	—	1	mA
			T _j = 125°C	—	—	10	

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Symbol	Parameter	Test Condition		Limits			Unit
				Min.	Typ.	Max.	
ID	Circuit Current	VD = 15V, V _{CIN} = 15V	V _{N1} -V _{NC}	—	45	62	mA
			V _{XP1} -V _{XPC}	—	15	20	
V _{th(on)}	Input ON Threshold Voltage	Applied between : UP-VUPC, VP-VVPC, WP-VWPC UN • VN • WN-VNC		1.2	1.5	1.8	V
V _{th(off)}	Input OFF Threshold Voltage			1.7	2.0	2.3	
OC	Over Current Trip Level	VD = 15V (Fig. 5,6)	T _J = 25°C	228	345	—	A
			T _J = 125°C	145	—	—	
SC	Short Circuit Trip Level	−20≤ T _J ≤ 125°C, VD = 15V (Fig. 5,6)		—	340	—	A
t _{off(OC)}	Over Current Delay Time	VD = 15V (Fig. 5,6)		—	10	—	μs
OT	Over Temperature Protection	Base-plate	Trip level	111	118	125	°C
OT _r		Temperature detection, VD = 15V	Reset level	—	100	—	
UV	Supply Circuit Under-Voltage Protection	−20 ≤ T _J ≤ 125°C	Trip level	11.5	12.0	12.5	V
UV _r			Reset level	—	12.5	—	
I _{FO(H)}	Fault Output Current	VD = 15V, V _{FO} = 15V (Note-3)	—	—	0.01	mA	
I _{FO(L)}			—	10	15		
t _{FO}	Minimum Fault Output Pulse Width	VD = 15V (Note-3)	1.0	1.8	—	ms	

(Note-3) Fault output is given only when the internal OC, SC, OT & UV protection.
 Fault output of OC, SC and UV protection operate by upper and lower arms.
 Fault output of OT protection operate by lower arm.
 Fault output of OC, SC protection given pulse.
 Fault output of OT, UV protection given pulse while over level.

MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Main terminal screw : M5	2.5	3.0	3.5	N • m
—	Mounting torque	Mounting part screw : M5	2.5	3.0	3.5	N • m
—	Weight	—	—	920	—	g

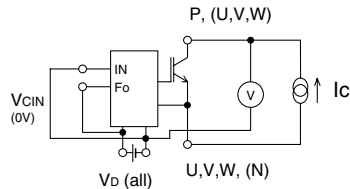
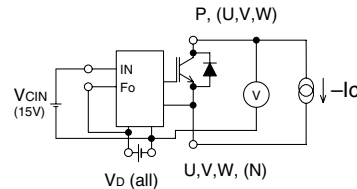
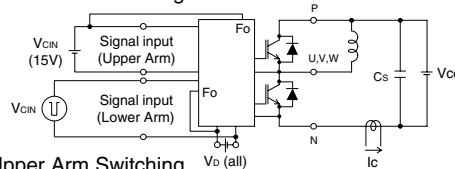
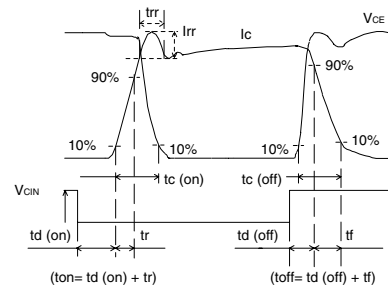
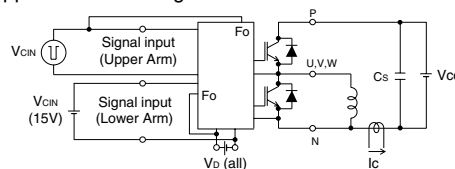
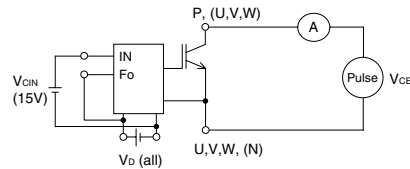
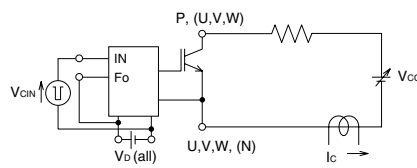
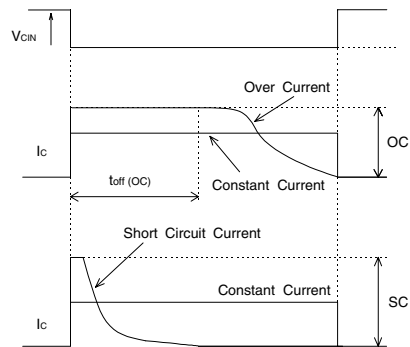
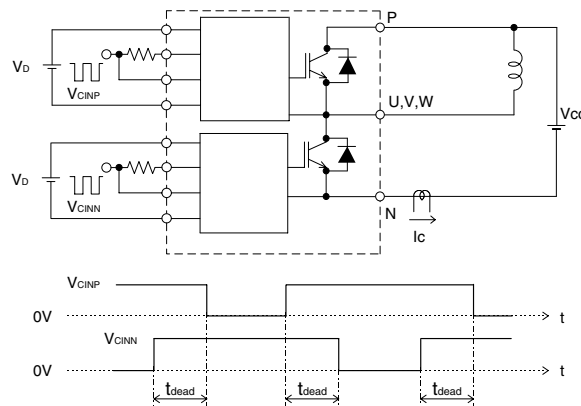
RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Test Condition	Recommended value	Unit
V _{CC}	Supply Voltage	Applied across P-N terminals	≤ 800	V
V _D	Control Supply Voltage	Applied between : VUP1-VUPC, VVP1-VVPC VWP1-VWPC, VN1-VNC (Note-4)	15 ± 1.5	V
V _{CIN(on)}	Input ON Voltage	Applied between : UP-VUPC, VP-VVPC, WP-VWPC UN • VN • WN-VNC	≤ 0.8	V
V _{CIN(off)}	Input OFF Voltage		≥ 4.0	
f _{PWM}	PWM Input Frequency	Using Application Circuit input signal of IPM, 3φ sinusoidal PWM VVVF inverter (Fig. 8)	≤ 20	kHz
t _{dead}	Arm Shoot-through Blocking Time	For IPM's each input signals (Fig. 7)	≥ 3.0	μs

(Note-4) Allowable Ripple rating of Control Voltage : dv/dt ≤ ±5V/μs, 2V_{p-p}

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- Before applying any control supply voltage (V_D), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.
After this, the specified ON and OFF level setting for each input signal should be done.
- When performing "OC" and "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
(These test should not be done by using a curve tracer or its equivalent.)

**Fig. 1 $V_{CE(sat)}$ Test****Fig. 2 V_{EC} Test****a) Lower Arm Switching****b) Upper Arm Switching****Fig. 3 Switching time Test circuit and waveform****Fig. 4 I_{CES} Test****Fig. 5 OC and SC Test****Fig. 6 OC and SC Test waveform****Fig. 7 Dead time measurement point example**

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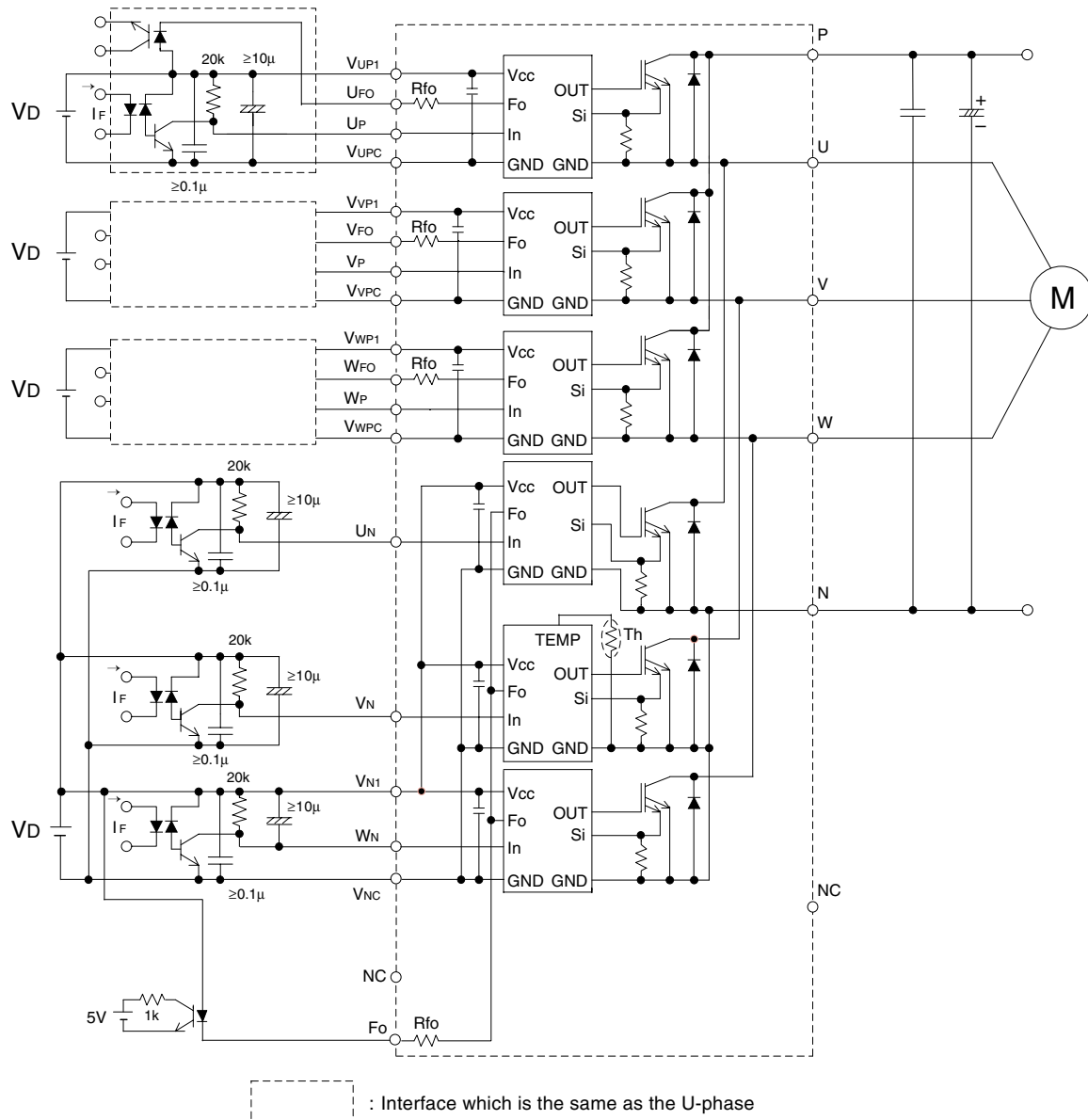


Fig. 8 Application Example Circuit

NOTES FOR STABLE AND SAFE OPERATION ;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Quick opto-couplers : $T_{PLH}, T_{PHL} \leq 0.8\mu s$. Use High CMR type. The line between opto-coupler and intelligent module should be shortened as much as possible to minimize the floating capacitance.
- Slow switching opto-coupler : recommend to use at $CTR = 100 \sim 200\%$, Input current = $8 \sim 10mA$, to work in active.
- Use 4 isolated control power supplies (VD). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. $4.7nF$) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.