

PS21245-E

TRANSFER-MOLD TYPE
INSULATED TYPE

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INTEGRATED POWER FUNCTIONS

4th generation (planar) IGBT inverter bridge for 3 phase DC-to-AC power conversion.

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

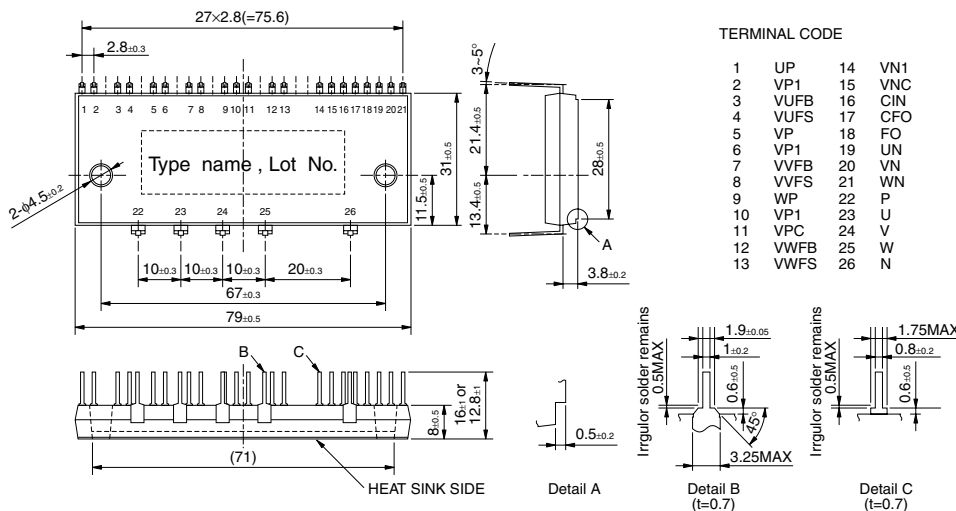
- For upper-leg IGBTs : Drive circuit, High voltage isolated high-speed level shifting, Control circuit under-voltage (UV) protection.
Note : Bootstrap supply scheme can be applied.
- For lower-leg IGBTs : Drive circuit, Control circuit under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling : Corresponding to a SC fault (Low-side IGBT) or a UV fault (Low-side supply).
- Input interface : 5V line CMOS/TTL compatible, Schmitt Trigger receiver circuit.

APPLICATION

AC100V~200V three-phase inverter drive for small power motor control.

Fig. 1 PACKAGE OUTLINES

Dimensions in mm



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Fig. 2 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)

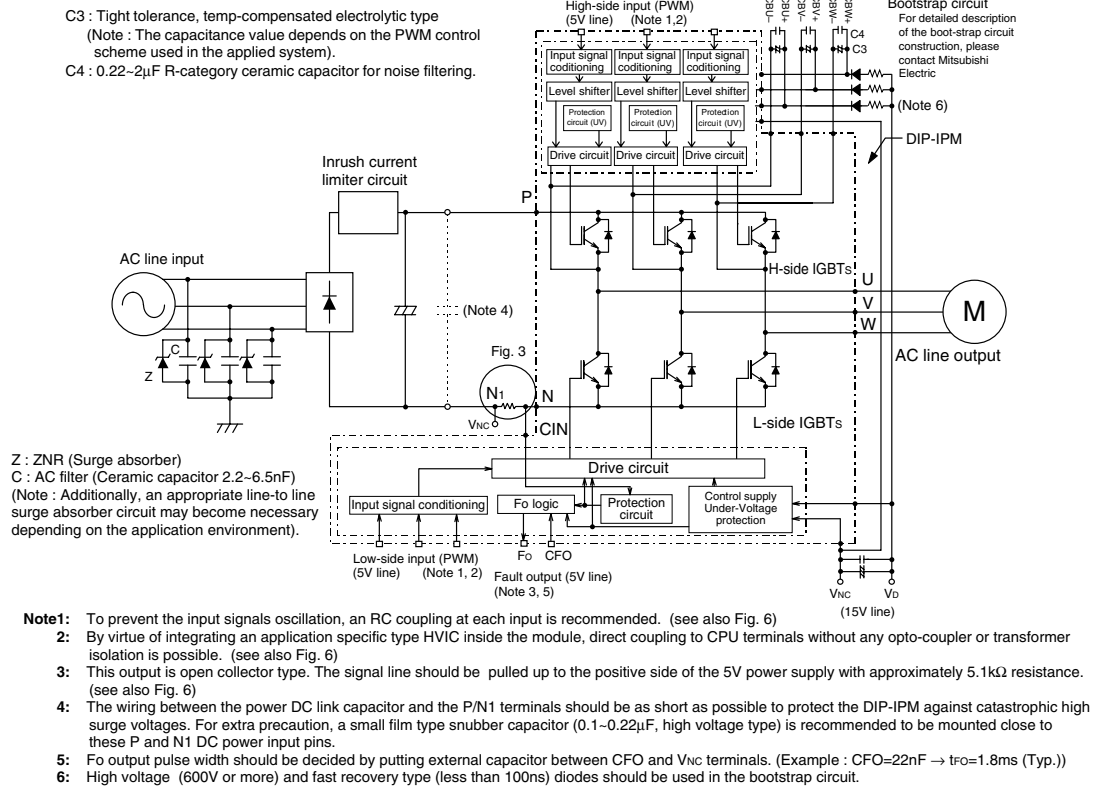
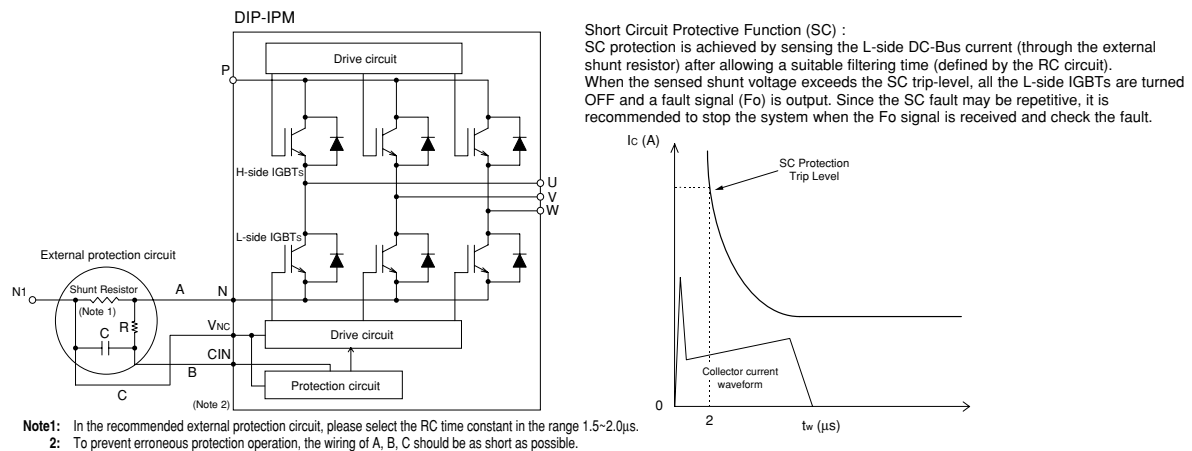


Fig. 3 EXTERNAL PART OF THE DIP-IPM PROTECTION CIRCUIT



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MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V _{CC}	Supply voltage	Applied between P-N	450	V
V _{CC(surge)}	Supply voltage (surge)	Applied between P-N	500	V
V _{CES}	Collector-emitter voltage		600	V
$\pm I_C$	Each IGBT collector current	$T_c = 25^\circ\text{C}$	20	A
$\pm I_{CP}$	Each IGBT collector current (peak)	$T_c = 25^\circ\text{C}$, instantaneous value (pulse)	40	A
P _C	Collector dissipation	$T_c = 25^\circ\text{C}$, per 1 chip	56	W
T _j	Junction temperature	(Note 1)	-20~+150	°C

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C ($@ T_c \leq 100^\circ\text{C}$) however, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to $T_{j(\text{ave})} \leq 125^\circ\text{C}$ ($@ T_c \leq 100^\circ\text{C}$).

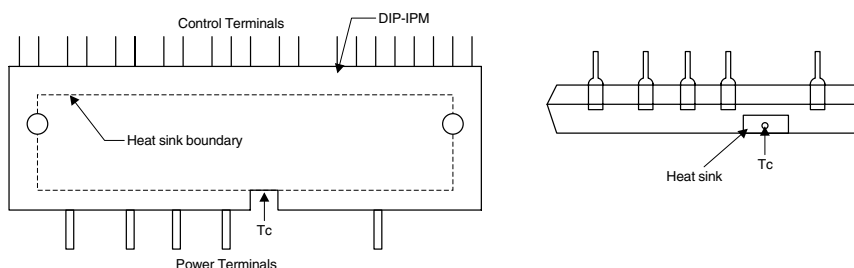
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V _D	Control supply voltage	Applied between VP1-VPC, VN1-VNC	20	V
V _{DB}	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	20	V
V _{CIN}	Input voltage	Applied between UP, VP, WP-VPC, UN, VN, WN-VNC	-0.5~+5.5	V
V _{FO}	Fault output supply voltage	Applied between FO-VNC	-0.5~V _D +0.5	V
I _{FO}	Fault output current	Sink current at FO terminal	15	mA
V _{SC}	Current sensing input voltage	Applied between CIN-VNC	-0.5~V _D +0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
V _{CC(prot)}	Self protection supply voltage limit (short circuit protection capability)	V _D = 13.5~16.5V, Inverter part $T_j = 125^\circ\text{C}$, non-repetitive, less than 2 μs	400	V
T _C	Module case operation temperature	(Note 2)	-20~+100	°C
T _{stg}	Storage temperature		-40~+125	°C
V _{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1 minute, connection pins to heat-sink plate	1500	V _{rms}

Note 2 : T_C MEASUREMENT POINT



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THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistance	Inverter IGBT part (per 1/6 module)	—	—	2.2	°C/W
$R_{th(j-c)F}$		Inverter FWD part (per 1/6 module)	—	—	4.5	°C/W
$R_{th(c-f)}$	Contact thermal resistance	Case to fin, (per 1 module) thermal grease applied	—	—	0.067	°C/W

ELECTRICAL CHARACTERISTICS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D = V_{DB} = 15\text{V}$ $V_{CIN} = 0\text{V}$	—	1.55	2.15	V
V_{EC}	FWD forward voltage	$T_j = 25^\circ\text{C}$, $-I_C = 20\text{A}$, $V_{CIN} = 5\text{V}$	—	2.20	3.00	V
t_{on}	Switching times	$V_{CC} = 300\text{V}$, $V_D = V_{DB} = 15\text{V}$ $I_C = 20\text{A}$, $T_j = 125^\circ\text{C}$, $V_{CIN} = 5\text{V} \leftrightarrow 0\text{V}$ Inductive load (upper-lower arm)	0.10	0.80	1.30	μs
t_{rr}			—	0.10	—	μs
$t_{c(on)}$			—	0.50	0.90	μs
t_{off}			—	1.60	2.60	μs
$t_{c(off)}$			—	1.00	1.90	μs
I_{CES}	Collector-emitter cut-off current	$V_{CE} = V_{CES}$	—	—	1	mA
		$T_j = 125^\circ\text{C}$	—	—	10	

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
V _D	Control supply voltage	Applied between V _{P1} -V _{PC} , V _{N1} -V _{NC}		13.5	15.0	16.5	V
V _{DB}	Control supply voltage	Applied between V _{UFB} -V _{UFS} , V _{VFB} -V _{VFS} , V _{WFB} -V _{WFS}		13.5	15.0	16.5	V
I _D	Circuit current	V _D = V _{DB} = 15V, V _{CIN} = 5V	Total of V _{P1} -V _{PC} , V _{N1} -V _{NC} V _{UFB} -V _{UFS} , V _{VFB} -V _{VFS} , V _{WFB} -V _{WFS}	—	—	8.50 1.00	mA
V _{FOH}	Fault output voltage	V _{SC} = 0V, F _O = 10kΩ 5V pull-up		4.9	—	—	
V _{FOL}		V _{SC} = 1V, F _O = 10kΩ 5V pull-up		—	0.8	1.2	V
V _{FOsat}		V _{SC} = 1V, I _{FO} = 15mA		0.8	1.2	1.8	V
t _{dead}	Arm shoot-through blocking time	Relates to corresponding input signal for blocking arm shoot-through. −20°C ≤ T _C ≤ 100°C		2.5	—	—	μs
V _{SC(ref)}	Short circuit trip level	T _J = 25°C, V _D = 15V (Note 3)		0.45	0.5	0.55	V
UV _{DBt}	Supply circuit under-voltage protection	T _J ≤ 125°C	Trip level	10.0	—	12.0	V
UV _{DBr}			Reset level	10.5	—	12.5	V
UV _{Dt}			Trip level	10.3	—	12.5	V
UV _{Dr}			Reset level	10.8	—	13.0	V
t _{FO}	Fault output pulse width	C _{FO} = 22nF (Note 4)		1.0	1.8	—	ms
V _{th(on)}	ON threshold voltage	Applied between : U _P , V _P , W _P -V _{PC} , U _N , V _N , W _N -V _{NC}		0.8	1.4	2.0	V
V _{th(off)}	OFF threshold voltage			2.5	3.0	4.0	V

Note 3 : Short circuit protection is functioning only at the low-arms. Please select the value of the external shunt resistor such that the SC trip-level is less than 34 A.

4 : Fault signal is output when the low-arms short circuit or control supply under-voltage protective functions operate. The fault output pulse-width t_{FO} depends on the capacitance value of C_{FO} according to the following approximate equation : $C_{FO} = 12.2 \times 10^{-6} \times t_{FO} [\text{F}]$.

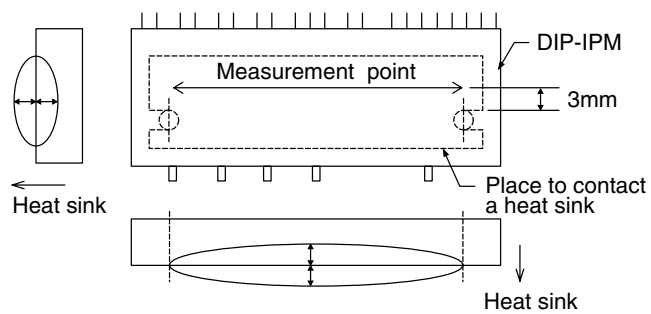
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MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M4	—	0.98	1.18	1.47	N·m
Terminal pulling strength	Weight 19.6N	EIAJ-ED-4701	10	—	—	s
Bending strength	Weight 9.8N. 90deg bend	EIAJ-ED-4701	2	—	—	times
Weight		—	—	54	—	g
Heat-sink flatness	(Note 5)	—	-50	—	100	μm

Note 5: Measurement point of heat-sink flatness



RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply voltage	Applied between P-N	0	300	400	V
V _D	Control supply voltage	Applied between VP1-VPC, VN1-VNC	13.5	15.0	16.5	V
V _{DB}	Control supply voltage	Applied between VUFB-VUFS, VVFB-VVFS, VWFB-VWFS	13.5	15.0	16.5	V
ΔV _D , ΔV _{DB}	Control supply variation		-1	—	1	V/μs
t _{dead}	Arm shoot-through blocking time	Relates to corresponding input signal for blocking arm shoot-through	2.5	—	—	μs
f _{PWM}	PWM input frequency	T _c ≤ 100°C, T _j ≤ 125°C	—	5	—	kHz
V _{CIN(ON)}	Input ON threshold voltage	Applied between UP, VP, WP-VPC	0~0.65			V
V _{CIN(OFF)}	Input OFF threshold voltage	Applied between UN, VN, WN-VNC	4.0~5.5			V

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Fig. 4 THE DIP-IPM INTERNAL CIRCUIT

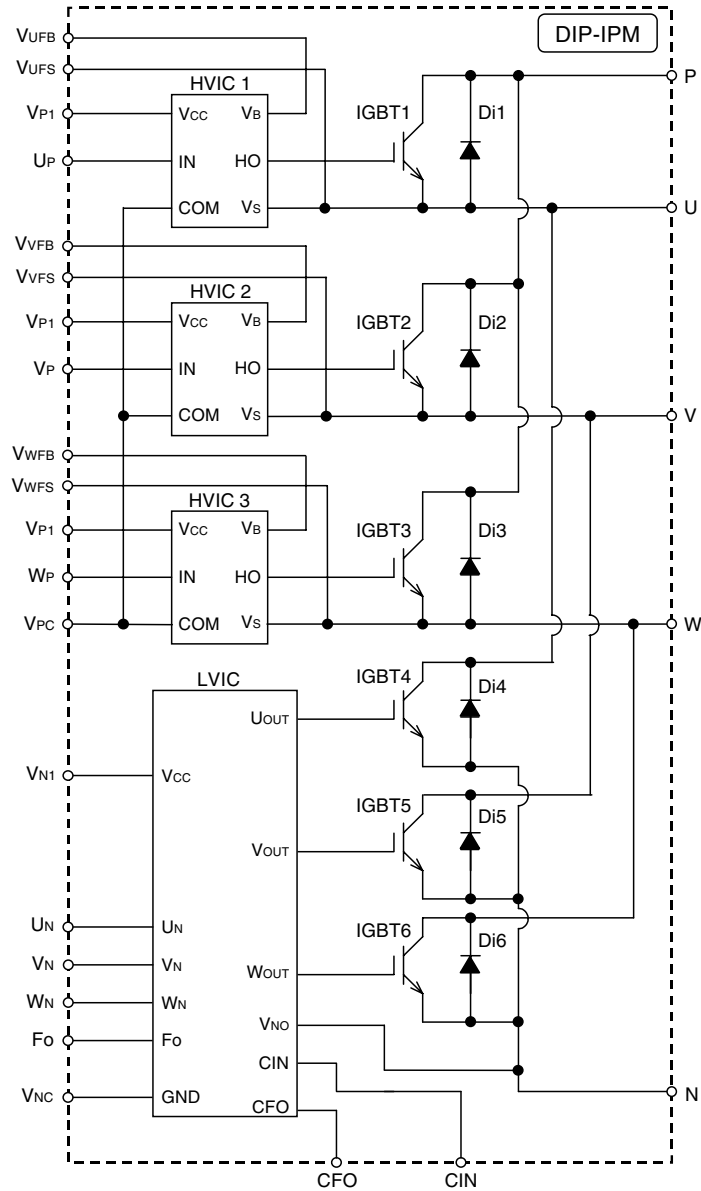


Fig. 5 TIMING CHARTS OF THE DIP-IPM PROTECTIVE FUNCTIONS
[A] Short-Circuit Protection (N-side only)

(For the external shunt resistor and CR connection.)

a1. Normal operation : IGBT ON and carrying current.

a2. Short circuit current detection (SC trigger).

a3. Hard IGBT gate interrupt.

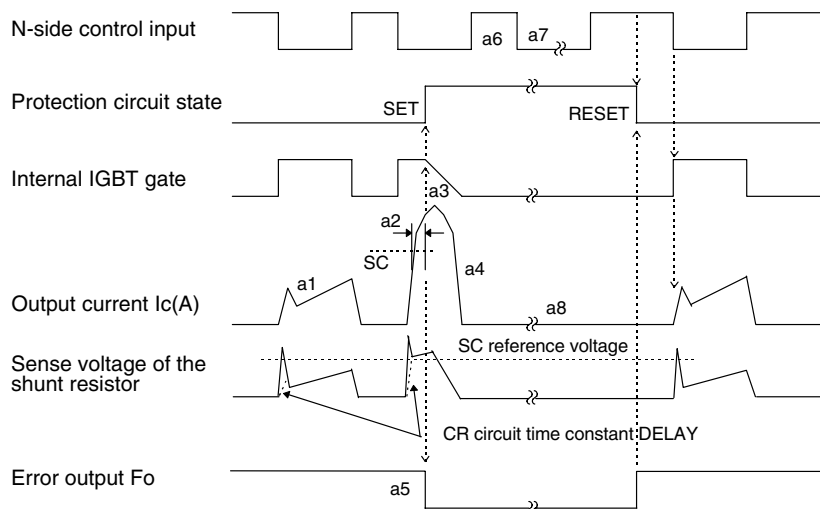
a4. IGBT turns OFF.

a5. Fo timer operation starts : The pulse width of the Fo signal is set by the external capacitor C_{FO}.

a6. Input "H" : IGBT OFF state.

a7. Input "L" : IGBT ON state.

a8. IGBT OFF state.


[B] Under-Voltage Protection (N-side, UV_D)

a1. Normal operation : IGBT ON and carrying current.

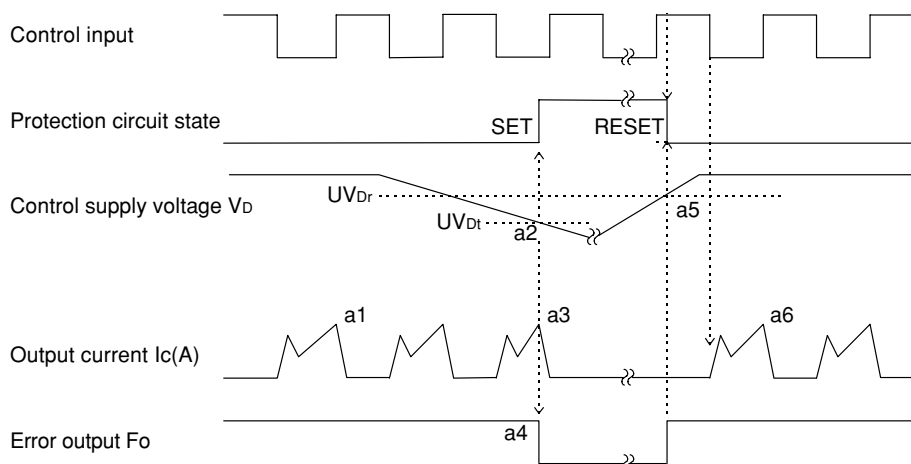
a2. Under voltage trip (UV_{Dt}).

a3. IGBT OFF in spite of control input condition.

a4. Fo timer operation starts.

a5. Under voltage reset (UV_{Dr}).

a6. Normal operation : IGBT ON and carrying current.



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[C] Under-Voltage Protection (P-side, UVDB)

- a1. Control supply voltage rises : After the voltage level reaches UVDBr, the circuits start to operate when the next input is applied.
- a2. Normal operation : IGBT ON and carrying current.
- a3. Under voltage trip (UVDBt).
- a4. IGBT OFF in spite of control input condition, but there is no Fo signal output.
- a5. Under-voltage reset (UVDBr).
- a6. Normal operation : IGBT ON and carrying current.

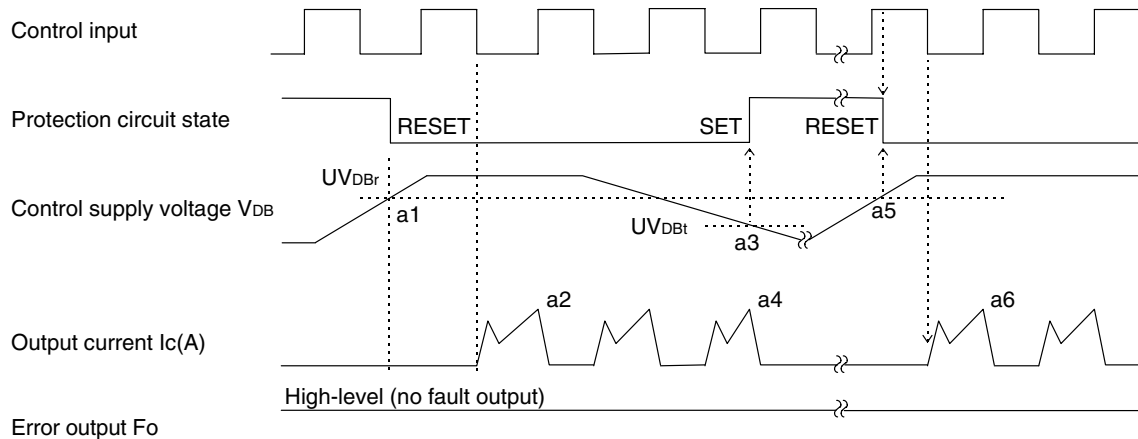
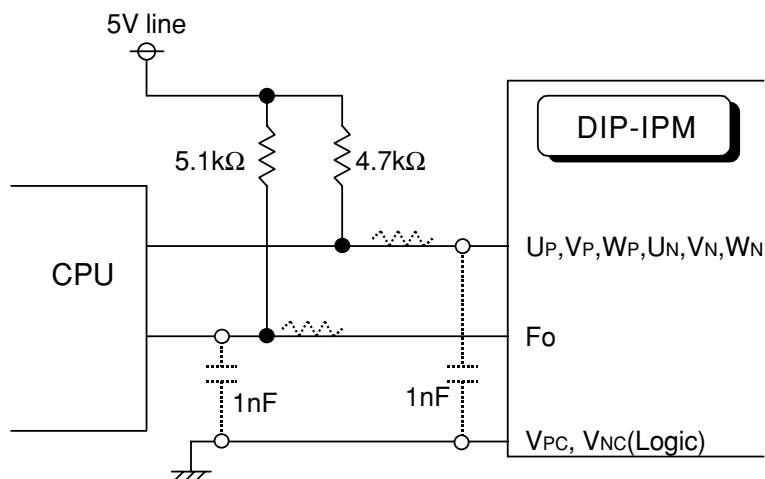


Fig. 6 RECOMMENDED CPU I/O INTERFACE CIRCUIT

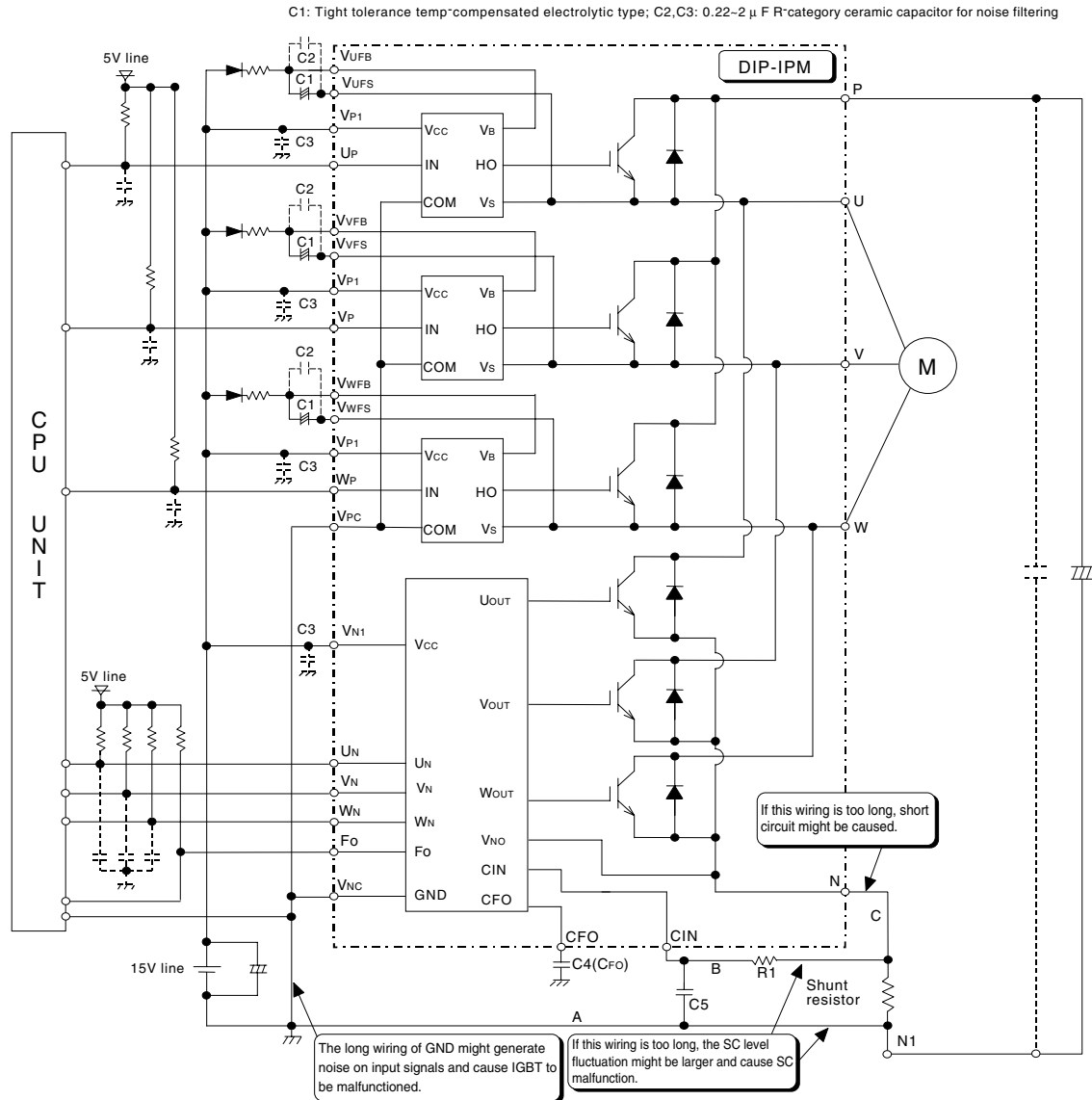


Note : RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and on the wiring impedances of the application's printed circuit board.

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Fig. 7 TYPICAL DIP-IPM APPLICATION CIRCUIT EXAMPLE



- Note 1 :** To prevent the input signals oscillation, an RC coupling at each input is recommended, and the wiring of each input should be as short as possible. (Less than 2cm)
- 2 :** By virtue of integrating an application specific type HVIC inside the module, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.
- 3 :** Fo output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 5.1k Ω resistance.
- 4 :** Fo output pulse width should be decided by connecting an external capacitor between CFC and VNC terminals (CFC). (Example : CFC = 22 nF $\rightarrow$ tFO = 1.8 ms (typ.))
- 5 :** Each input signal line should be pulled up to the 5V power supply with approximately 4.7k Ω resistance (other RC coupling circuits at each input may be needed depending on the PWM control scheme used and on the wiring impedances of the system's printed circuit board). Approximately a 0.22~2 μ F by-pass capacitor should be used across each power supply connection terminals.
- 6 :** To prevent errors of the protection function, the wiring of A, B, C should be as short as possible.
- 7 :** In the recommended protection circuit, please select the R1C5 time constant in the range 1.5~2 μ s.
- 8 :** Each capacitor should be put as nearby the pins of the DIP-IPM as possible.
- 9 :** To prevent surge destruction, the wiring between the smoothing capacitor and the P&N1 pins should be as short as possible. Approximately a 0.1~0.22 μ F snubber capacitor between the P&N1 pins is recommended.