RM5261A

RM5261A™ Microprocessor with 64-Bit System Bus

Data Sheet

Proprietary and Confidential

Preliminary

Issue 3, February 2002

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Revision History

Issue No.	Issue Date	Details of Change
3	January 2002	Modified features to include 400 MHz operating frequency, 560 Dhrystone MIPS, and 800 MFLOPS. Modified system interface description (page 21) to read a peak rate of 1 GByte/sec with 125 MHz SysClock. Modified recommended operating conditions table (page 31), power consumption table (page 33), clock parameters table (page 34), and system interface parameters table (page 35) to include values for 400 MHz operation. Added RM5261A-400-H to the valid combinations.
2	August 2001	Added 1.8 V to the feature: 1.65 V or 1.8 V core with 3.3 V or 2.5 V I/O (p9). Changed recommended operating conditions VccInt to 1.57 V to 1.85 V and VccP to 1.57 V to 1.85 V. Added VssP commercial and industrial values. Modified Note 4. Added reference to VccInt to Power Consumption table. Changed standby modes to 350. Changed maximum worst case instruction mix to 1250. Modified Note 1. Modified SysClock Frequency and SysClock Period values in the Clock Parameters table.
1	March 2001	Applied PMC-Sierra template to existing MPD (QED) FrameMaker document. Revised features list, Absolute Maximum Ratings table, Recommended Operating Conditions table, DC Electrical Characteristics table, Power Consumption table, Clock Parameters table and the System Interface Parameters table.

Document Conventions

The following conventions are used in this datasheet:

- All signal, pin, and bus names described in the text, such as **ExtRqst*,** are in boldface typeface.
- All bit and field names described in the text, such as ***Interrupt Mask***, are in an italic-bold typeface.
- All instruction names, such as MFHI, are in san serif typeface.

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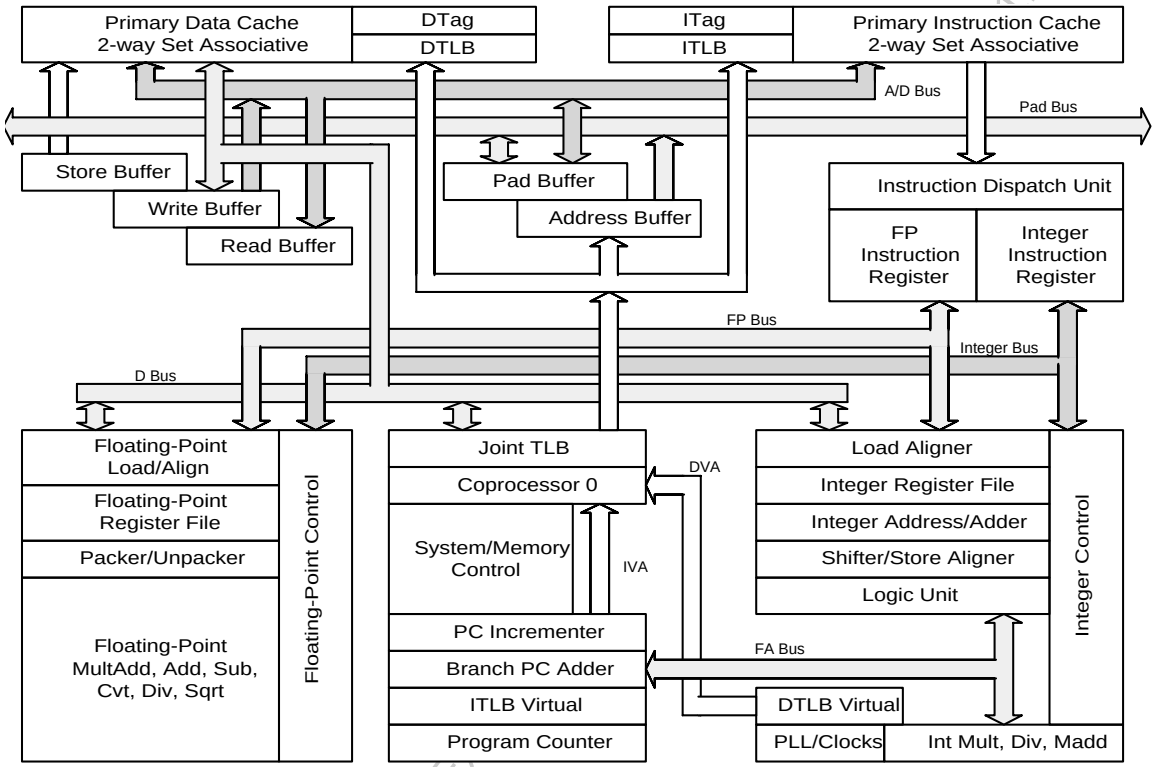
1 Features

- Dual Issue superscalar microprocessor
  - 250, 300, 350, and 400 MHz operating frequencies
  - Up to 560 Dhrystone 2.1 MIPS
- High-performance system interface
  - 64-bit multiplexed system address/data bus for optimum price/performance
  - High-performance write protocols maximize uncached write bandwidth
  - Processor clock multipliers 2, 2.5, 3, 3.5, 4, 4.5, 5, 6, 7, 8, 9
  - IEEE 1149.1 JTAG boundary scan
- Integrated on-chip caches
  - 32 KB instruction and 32 KB data — 2 way set associative
  - Per set locking
  - Virtually indexed, physically tagged
  - Write-back and write-through on a per page basis
  - Pipeline restart on first doubleword for data cache misses
- Integrated memory management unit
  - Fully associative joint TLB (shared by I and D translations)
  - 48 dual entries map 96 pages
  - Variable page size (4 KB to 16 MB in 4x increments)
- High-performance floating-point unit: up to 800 MFLOPS
  - Single cycle repeat rate for common single-precision operations and some double-precision operations
  - Two cycle repeat rate for double-precision multiply and double precision combined multiply-add operations
  - Single cycle repeat rate for single-precision combined multiply-add operation
- MIPS IV instruction set
  - Floating point multiply-add instruction increases performance in signal processing and graphics applications
  - Conditional moves to reduce branch frequency
  - Index address modes (register + register)
- Embedded application enhancements
  - Specialized DSP integer Multiply-Accumulate instructions and 3-operand multiply instruction
  - I and D cache locking by set
  - Optional dedicated exception vector for interrupts
- Fully static 0.18 micron CMOS design with power down logic
  - Standby reduced power mode with WAIT instruction
  - 1.65 V or 1.8 V core with 3.3 V or 2.5 V I/O
- 208-pin QFP package

2 Block Diagram

Figure 1 Block Diagram



3 Hardware Overview

The RM5261A offers a high-level of integration targeted at high-performance embedded applications. The key elements of the RM5261A are briefly described below.

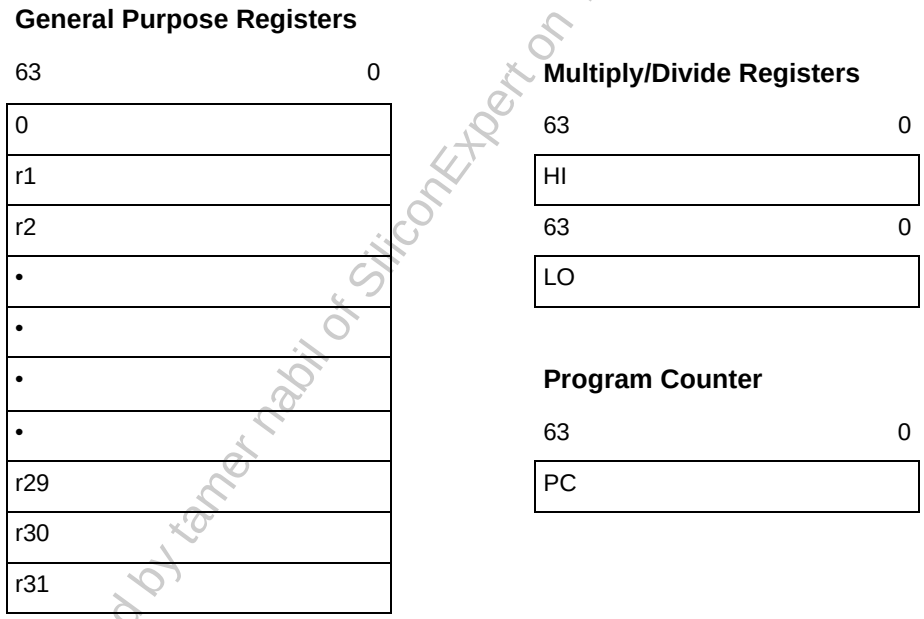
3.1 Superscalar Dispatch

The RM5261A has an asymmetric superscalar dispatch unit which allows it to issue an integer instruction and a floating-point computation instruction simultaneously. Integer instructions include alu, branch, load/store, and floating-point load/store, while floating-point computation instructions include floating-point add, subtract, combined multiply-add, and convert. In combination with its high-throughput fully pipelined floating-point execution unit, the superscalar capability of the RM5261A provides unparalleled price/performance in computationally intensive embedded applications.

3.2 CPU Registers

The RM5261A CPU contains 32 general purpose registers, two special purpose registers for integer multiplication and division, a program counter, and no condition code bits. Figure 2 shows the user visible state.

Figure 2 CPU Registers



3.3 Integer Unit

The RM5261A implements the MIPS IV Instruction Set Architecture and is therefore fully upward compatible with applications that run on processors implementing the earlier generation MIPS I-III instruction sets. Additionally, the RM5261A includes two implementation specific instructions not found in the baseline MIPS IV ISA but that are useful in the embedded market place. These instructions are integer multiply-accumulate (MAD) and 3-operand integer multiply (MUL).

The RM5261A integer unit includes thirty-two general purpose 64-bit registers, a load/store architecture with single cycle ALU operations (add, sub, logical, shift) and an autonomous multiply/divide unit. Additional register resources include: the HI/LO result registers for the two-operand integer multiply/divide operations, and the program counter (PC).

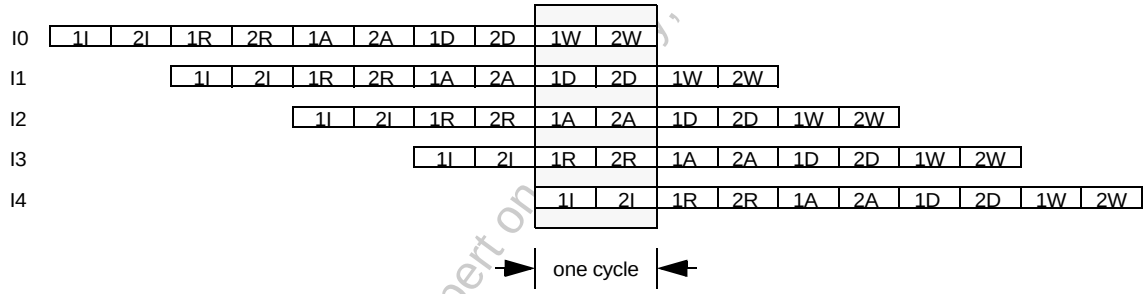
3.4 Pipeline

For integer operations, loads, stores, and other non-floating-point operations, the RM5261A implements a 5-stage integer pipeline. In addition to the integer pipeline, the RM5261A implements an extended 7-stage pipeline for floating-point operations.

The RM5261A multiplies the input SysClock by 2, 2.5, 3, 3.5, 4, 4.5, 5, 6, 7, 8, or 9 to produce the pipeline clock.

Figure 3 shows the RM5261A integer pipeline. As illustrated in the figure, up to five integer instructions can be executing simultaneously.

Figure 3 Pipeline



1I-1R: Instruction cache access
2I: Instruction virtual to physical address translation
2R: Register file read, Bypass calculation, Instruction decode, Branch address calculation
1A: Issue or slip decision, Branch decision
1A: Data virtual address calculation
1A-2A: Integer add, logical, shift
2A: Store Align
2A-2D: Data cache access and load align
1D: Data virtual to physical address translation
2W: Register file write

3.5 Register File

The RM5261A has thirty-two general purpose registers with register location 0 (r0) hard-wired to a zero value. These registers are used for scalar integer operations and address calculation. The register file has two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

3.6 ALU

The RM5261A ALU consists of an integer adder/subtractor, a logic unit, and a shifter. The adder performs address calculations in addition to arithmetic operations. The logic unit performs all logical and zero shift data moves. The shifter performs shifts and store alignment operations. Each of these units is optimized to perform all operations in a single processor cycle.

3.7 Integer Multiply/Divide

The RM5261A has a dedicated integer multiply/divide unit optimized for high-speed multiply and multiply-accumulate operations. Table 1 shows the performance of the multiply/divide unit on each operation.

Table 1 Integer Multiply/Divide Operations

Opcode	Operand Size	Latency	Repeat Rate	Stall Cycles
MULT/U, MAD/U	16 bit	3	2	0
	32 bit	4	3	0
MUL	16 bit	3	2	1
	32 bit	4	3	2
DMULT, DMULTU	any	7	6	0
DIV, DIVD	any	36	36	0
DDIV, DDIVU	any	68	68	0

The baseline MIPS IV ISA specifies that the results of a multiply or divide operation be placed in the Hi and Lo registers. These values can then be transferred to the general purpose register file using the Move-from-Hi and Move-from-Lo (MFHI/MFLO) instructions.

In addition to the baseline MIPS IV integer multiply instructions, the RM5261A also implements the 3-operand multiply instruction, MUL. This instruction specifies that the multiply result go directly to the integer register file rather than the Lo register. The portion of the multiply that would have normally gone into the Hi register is discarded. For applications where it is known that the upper half of the multiply result is not required, using the MUL instruction eliminates the necessity of executing an explicit MFLO instruction.

The multiply-add instructions, MAD and MADU, multiply two operands and add the resulting product to the current contents of the Hi and Lo registers. The multiply-accumulate operation is the core primitive of almost all signal processing algorithms, allowing the RM5261A to eliminate the need for a separate DSP engine in many embedded applications.

3.8 Floating-Point Co-Processor

The RM5261A incorporates a high-performance fully pipelined floating-point co-processor which includes a floating-point register file and autonomous execution units for multiply/add/convert and divide/square root. The floating-point coprocessor is a tightly coupled execution unit, decoding and executing instructions in parallel with, and in the case of floating-point loads and stores, in cooperation with the integer unit. The superscalar capabilities of the RM5261A allow floating-point computation instructions to issue concurrently with integer instructions.

3.9 Floating-Point Unit

The RM5261A floating-point execution unit supports single and double precision arithmetic, as specified in the IEEE Standard 754. The execution unit is broken into a separate divide/square root

unit and a pipelined multiply/add unit. Overlap of the divide/square root and multiply/add operations is supported.

The RM5261A maintains fully precise floating-point exceptions while allowing both overlapped and pipelined operations. Precise exceptions are extremely important in object-oriented programming environments and highly desirable for debugging in any environment.

Floating-point operations include:

- add
- subtract
- multiply
- divide
- square root
- reciprocal
- reciprocal square root
- conditional moves
- conversion between fixed-point and floating-point format
- conversion between floating-point formats
- floating-point compare

Table 2 gives the latencies of the floating-point instructions in internal processor cycles.

Table 2 Floating-Point Instruction Cycles

Operation	Latency	Repeat Rate
fadd	4	1
fsub	4	1
fmult	4/5	1/2
fmadd	4/5	1/2
fmsub	4/5	1/2
fdiv	21/36	19/34
fsqrt	21/36	19/34
frecip	21/36	19/34
frsqrt	38/68	36/66
fcvt.s.d	4	1
fcvt.s.w	6	3
fcvt.s.l	6	3
fcvt.d.s	4	1
fcvt.d.w	4	1

Operation	Latency	Repeat Rate
fcvt.d.l	4	1
fcvt.w.s	4	1
fcvt.w.d	4	1
fcvt.l.s	4	1
fcvt.l.d	4	1
fcmp	1	1
fmov	1	1
fmovc	1	1
fabs	1	1
fneg	1	1

Notes:

1. Numbers are represented as single/double precision format.

3.10 Floating-Point General Register File

The floating-point general register file (FGR) is made up of thirty-two 64-bit registers. With the floating-point load and store double instructions (LDC1 and SDC1) the floating-point unit can take advantage of the 64-bit wide data cache and issue a floating-point coprocessor load or store doubleword instruction in every cycle.

The floating-point control register space contains two registers; one for determining configuration and revision information for the coprocessor, and one for control and status information. These are primarily used for diagnostic software, exception handling, state saving and restoring, and control of rounding modes. To support superscalar operation, the FGR has four read ports and two write ports, and is fully bypassed to minimize operation latency in the pipeline. Three of the read ports and one write port are used to support the combined multiply-add instruction while the fourth read and second write port allows a concurrent floating-point load or store.

3.11 System Control Co-processor (CP0)

The system control coprocessor, also called coprocessor 0 or CP0 in the MIPS architecture, is responsible for the virtual memory sub-system, the exception control system, and the diagnostics capability of the processor. In the MIPS architecture, the system control co-processor (and thus the kernel software) is implementation dependent.

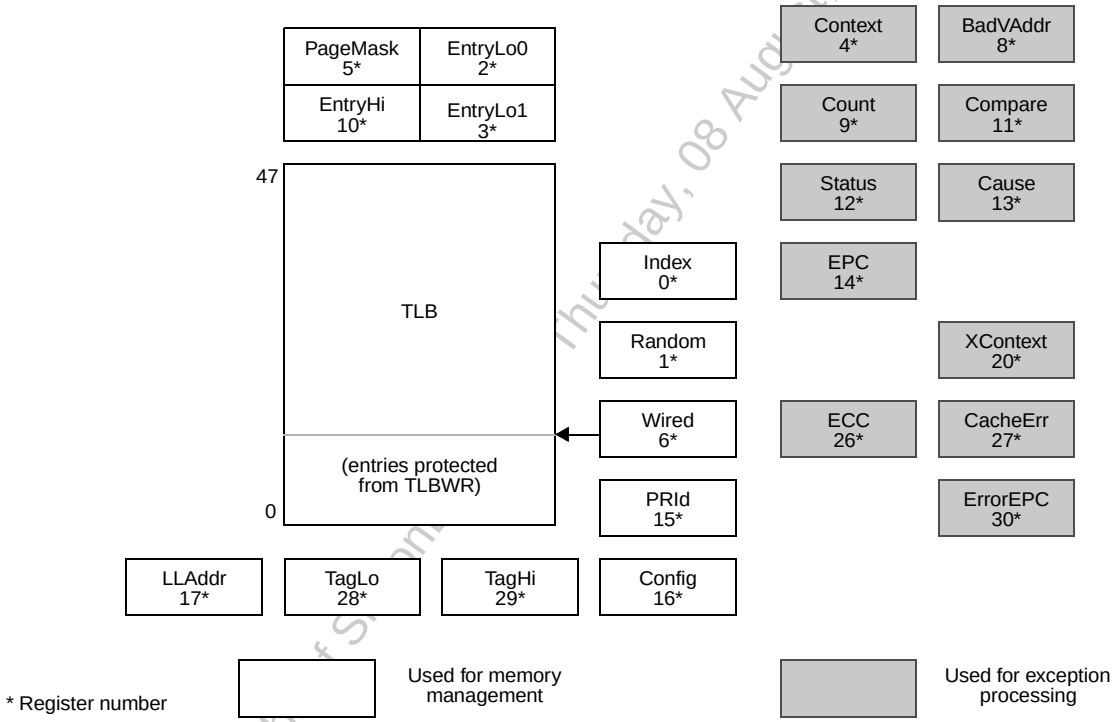
The memory management unit controls the virtual memory system page mapping. It consists of an instruction address translation buffer, ITLB, a data address translation buffer, DTLB, a Joint instruction and data address translation buffer, JTLB, and co-processor registers used by the virtual memory mapping sub-system.

3.12 System Control Co-Processor Registers

The RM5261A incorporates all system control co-processor (CP0) registers on-chip. These registers provide the path through which the virtual memory system's page mapping is examined and modified, exceptions are handled, and operating modes are controlled (kernel vs. user mode, interrupts enabled or disabled, cache features). In addition, the RM5261A includes registers to implement a real-time cycle counting facility to aid in cache diagnostic testing and to assist in data error detection.

Figure 4 shows the CP0 registers.

Figure 4 CP0 Registers



3.13 Virtual to Physical Address Mapping

The RM5261A provides three modes of virtual addressing:

- user mode
- kernel mode
- supervisor mode

This mechanism allows system software to provide a secure environment for user processes. Bits in the CP0 register Status determine which virtual addressing mode is used. In the user mode, the RM5261A provides a single, uniform virtual address space of 1 TB (2 GB in 32-bit mode).

When operating in the kernel mode, four distinct virtual address spaces, totalling over 2.5 TB (4 GB in 32-bit mode), are simultaneously available and are differentiated by the high-order bits of the virtual address.

The RM5261A processors also support a supervisor mode in which the virtual address space over 2 TB (2.5 GB in 32-bit mode), divided into three regions based on the high-order bits of the virtual address.

When the RM5261A is configured as a 64-bit microprocessor, the virtual address space layout is an upward compatible extension of the 32-bit virtual address space layout.

Figure 5 shows the address space layout for 32-bit operation

Figure 5 Kernel Mode Virtual Addressing (32-bit)

0xFFFFFFFF	Kernel virtual address space
	(kseg3)
0xE0000000	Mapped, 0.5GB
0xDFFFFFFF	Supervisor virtual address space
	(ksseg)
0xC0000000	Mapped, 0.5GB
0xBFFFFFFF	Uncached kernel physical address space
	(kseg1)
0xA0000000	Unmapped, 0.5GB
0x9FFFFFFF	Cached kernel physical address space
	(kseg0)
0x80000000	Unmapped, 0.5GB
0x7FFFFFFF	User virtual address space
	(kuseg)
	Mapped, 2.0GB
0x00000000	

3.14 Joint TLB

For fast virtual-to-physical address translation, the RM5261A uses a large, fully associative TLB that maps 96 virtual pages to their corresponding physical addresses. As indicated by its name, the joint TLB (JTLB) is used for both instruction and data translations. The JTLB is organized as 48 pairs of even-odd entries, and maps a virtual address and address space identifier into the large, 64 GB physical address space.

Two mechanisms are provided to assist in controlling the amount of mapped space and the replacement characteristics of various memory regions. First, the page size can be configured, on a per-entry basis, to use page sizes in the range of 4 KB to 16 MB (in multiples of 4). The CP0 Page Mask register is loaded with the desired page size of a mapping, and that size is stored into the

TLB along with the virtual address when a new entry is written. Thus, operating systems can create special purpose maps; for example, an entire frame buffer can be memory mapped using only one TLB entry.

The second mechanism controls the replacement algorithm when a TLB miss occurs. The RM5261A provides a random replacement algorithm to select a TLB entry to be written with a new mapping; however, the processor also provides a mechanism whereby a system specific number of mappings can be locked into the TLB, thereby avoiding random replacement. This mechanism uses the Wired register and allows the operating system to guarantee that certain pages are always mapped for performance reasons and for deadlock avoidance. This mechanism also facilitates the design of real-time systems by allowing deterministic access to critical software.

The JTLB also contains information that controls the cache coherency protocol for each page. Specifically, each page has attribute bits to determine whether the coherency algorithm is one of the following:

- uncached
- non-coherent write-back
- non-coherent write-through with write-allocate
- non-coherent write-through without write-allocate
- sharable
- exclusive
- update

The non-coherent protocols are used for both code and data on the RM5261A, with data using write-back or write-through depending on the application.

The coherency attributes generate coherent transaction types on the system interface. However, in the RM5261A cache coherency is not supported. Hence the coherency attributes should never be used.

3.15 Instruction TLB

The RM5261A implements a 2-entry instruction TLB (ITLB) to minimize contention for the JTLB, eliminate the timing critical path of translating through a large associative array, and save power. Each ITLB entry maps a 4 KB page. The ITLB improves performance by allowing instruction address translation to occur in parallel with data address translation. When a miss occurs on an instruction address translation by the ITLB, the least-recently used ITLB entry is filled from the JTLB. The operation of the ITLB is completely transparent to the user.

3.16 Data TLB

The RM5261A implements a 4-entry data TLB (DTLB) for the same reasons cited above for the ITLB. Each DTLB entry maps a 4 KB page. The DTLB improves performance by allowing data address translation to occur in parallel with instruction address translation. When a miss occurs on a data address translation by the DTLB, the DTLB is filled from the JTLB. The DTLB refill is pseudo-LRU: the least recently used entry of the least recently used pair of entries is filled. The operation of the DTLB is completely transparent to the user.

3.17 Cache Memory

The RM5261A incorporates on-chip instruction and data caches that can be accessed in a single processor cycle. Each cache has its own 64-bit data path and both caches can be accessed simultaneously. The cache subsystem provides the integer and floating-point units with an aggregate bandwidth of 3.2 GB per second at an internal clock frequency of 200 MHz.

3.18 Instruction Cache

The RM5261A incorporates a two-way set associative on-chip instruction cache. This virtually indexed, physically tagged cache is 32 KB in size and is protected with word parity.

Since the cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, further increasing performance by allowing these two operations to occur simultaneously. The cache tag contains a 24-bit physical address, a valid bit, and a single parity bit.

The instruction cache is 64-bits wide and can be accessed each processor cycle. Accessing 64 bits per cycle allows the instruction cache to supply two instructions per cycle to the superscalar dispatch unit. For typical code sequences where a floating-point load or store and a floating-point computation instruction are being issued together in a loop, the entire bandwidth available from the instruction cache is consumed.

Cache miss refill writes 64 bits per cycle to minimize the cache miss penalty. The line size is eight instructions (32 bytes) to maximize the performance of communication between the processor and the memory system.

The RM5261A supports cache locking. The contents of set A of the cache can be *locked* by setting a bit in the coprocessor 0 Status register. Locking the set prevents its contents from being overwritten by a subsequent cache miss. Refills occur only into set B. This mechanism allows the programmer to lock critical code into the cache, thereby guaranteeing deterministic behavior for the locked code sequence.

3.19 Data Cache

For fast, single cycle data access, the RM5261A includes a 32 KB on-chip data cache that is two-way set associative with a fixed 32-byte (eight words) line size.

The data cache is protected with byte parity and its tag is protected with a single parity bit. It is virtually indexed and physically tagged to allow simultaneous address translation and data cache access.

Cache protocols supported for the data cache are:

1. Uncached

   Data loads and instruction fetches from uncached memory space are brought in from the main memory to the register file and the execution unit, respectfully. The caches are not accessed. Data stores to uncached memory space go directly to the main memory without updating the data cache.

2. Write-back

   Loads and instruction fetches first search the cache, reading main memory only if the desired data is not cache resident. On data store operations, the cache is first searched to determine if

the target address is cache resident. If it is resident, the cache contents are updated, and the cache line is marked for later write-back. If the cache lookup misses, the target cache line is first brought into the cache and then the write is performed as above.

3. Write-through with write allocate

   Loads and instruction fetches first search the cache, reading main memory only if the desired data is not cache resident. On data store operations, the cache is first searched to determine if the target address is cache resident. If it is resident, the cache contents are updated and main memory is written, leaving the ***write-back*** bit of the cache line unchanged. If the cache lookup misses, the target line is first brought into the cache and then the write is performed as above.

4. Write-through without write allocate

   Loads and instruction fetches first search the cache, reading main memory only if the desired data is not cache resident. On data store operations, the cache is first searched to determine if the target address is cache resident. If it is resident, the cache contents are updated and main memory is written, leaving the ***write-back*** bit of the cache line unchanged. If the cache lookup misses, then only main memory is written.

The most commonly used write policy is write-back, where a store to a cache line does not immediately cause main memory to be updated. This increases system performance by reducing bus traffic and eliminating the bottleneck of waiting for each store operation to finish before issuing a subsequent memory operation. Software can, however, select write-through on a per-page basis when appropriate, such as for frame buffers.

Associated with the data cache is the store buffer. When the RM5261A executes a store instruction, this single-entry buffer gets written with the store data while the tag comparison is performed. If the tag matches, then the data is written into the data cache in the next cycle that the data cache is not accessed (the next non-load cycle). The store buffer allows the RM5261A to execute a store every processor cycle and to perform back-to-back stores without penalty. In the event of a store immediately followed by a load to the same address, a combined merge and cache write occurs such that no penalty is incurred. The RM5261A cache attributes for both the instruction and data caches are summarized in Table 3.

Table 3 Cache Attributes

Characteristics	Instruction	Data
Size	32KB	32KB
Organization	2-way set associative	2-way set associative
Line size	32B	32B
Index	$vAddr_{11..0}$	$vAddr_{11..0}$
Tag	$pAddr_{31..12}$	$pAddr_{31..12}$
Write policy	n.a.	write-back/write-through
Read order	sub-block	sub-block
Write order	sequential	sequential
miss restart after transfer of	entire line	first double
Parity	per-word	per-byte
Cache locking	set A	set A

3.20 Write buffer

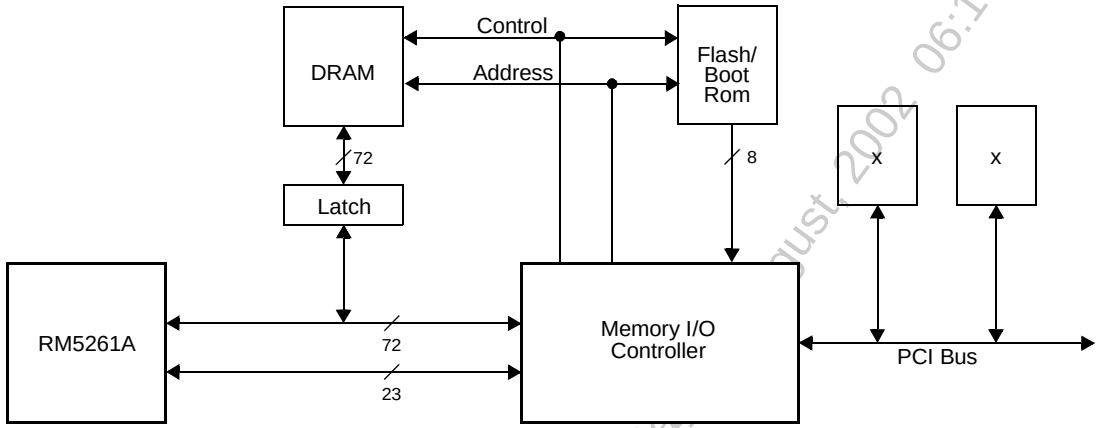
Writes to external memory, whether cache miss write-backs or stores to uncached or write-through addresses, use the on-chip write buffer. The write buffer holds up to four 64-bit address and data pairs. The entire buffer is used for a data cache write-back and allows the processor to proceed in parallel with the memory update. For uncached and write-through stores, the write buffer significantly increases performance by decoupling the **SysAD** bus transfers from the instruction execution stream.

3.21 System Interface

The system interface consists of a 64-bit Address/Data bus with 8 parity check bits and a 9-bit command bus. In addition, there are 6 handshake signals and 6 interrupt inputs. The interface is capable of transferring data between the processor and memory at a peak rate of 1 GB/sec with a 125 MHz SysClock.

Figure 6 shows a typical embedded system using the RM5261A. In this example, a bank of DRAMs and a memory controller ASIC share the processor's **SysAD** bus while the memory controller provides separate ports to a boot ROM and an I/O system.

Figure 6 Typical Embedded System Block Diagram



3.22 System Address/Data Bus

The 64-bit System Address Data (**SysAD**) bus is used to transfer addresses and data between the RM5261A and the rest of the system. It is protected with an 8-bit parity check bus (**SysADC)**. The system interface is configurable to allow easy interfacing to memory and I/O systems of varying frequencies.

The Block Write data rate, Non-block Write protocol, and the Output Drive strength are programmable at Boot time via the ***Mode Control*** bits. The rate at which the processor receives data is also fully controlled by the external device.

3.23 System Command Bus

The RM5261A interface has a 9-bit System Command (**SysCmd**) bus. The command bus indicates whether the **SysAD** bus carries address or data information on a per-clock basis. If the **SysAD** carries address, the **SysCmd** bus indicates what type of transaction is to take place (for example, a read or write). If the **SysAD** carries data, the **SysCmd** bus provides information about the data (for example, this is the last data word transmitted, or the data contains an error). The **SysCmd** bus is bidirectional to support both processor requests and external requests to the RM5261A. Processor requests are initiated by the RM5261A and responded to by an external device. External requests are issued by an external device and require the RM5261A to respond.

The RM5261A supports one- to eight-byte transfers as well as block transfers on the **SysAD** bus. In the case of a sub-double word transfer, the three low-order address bits give the byte address of the transfer, and the **SysCmd** bus indicates the number of bytes being transferred.

3.24 Handshake Signals

There are six handshake signals on the system interface. Two of these, **RdRdy*** and **WrRdy***, are used by an external device to indicate to the RM5261A whether it can accept a new read or write

transaction. The RM5261A samples these signals before deasserting the address on read and write requests.

ExtRqst* and **Release*** are used to transfer control of the **SysAD** and **SysCmd** buses from the processor to an external device. When an external device needs to control the interface, it asserts **ExtRqst***. The RM5261A responds by asserting **Release*** to release the system interface to slave state.

ValidOut* and **ValidIn*** are used by the RM5261A and the external device respectively to indicate that there is a valid address, a command, or data on the **SysAD** and **SysCmd** buses. The RM5261A asserts **ValidOut*** when it is driving these buses with a valid address, a command, or data, and the external device drives **ValidIn*** when it has control of the buses and is driving a valid address, a command, or data.

3.25 Non-overlapping System Interface

The RM5261A implements a non-overlapping system interface, meaning that only one processor request may be outstanding at a time and that the request must be serviced by an external device before the RM5261A issues another request. The RM5261A can issue read and write requests to an external device, whereas an external device can issue null and write requests to the RM5261A.

For processor reads the RM5261A asserts **ValidOut*** and simultaneously drives the address and read command on the **SysAD** and **SysCmd** buses respectively. If the system interface has **RdRdy*** asserted, then the processor tristates its drivers and releases the system interface to the slave state by asserting **Release***. The external device can then begin sending data to the RM5261A.

Figure 7 shows a processor block read request and the external agent read response. The read latency is 4 cycles (**ValidOut*** to **ValidIn***), and the response data pattern is DDDD, indicating that data can be transferred on every clock with no wait states in-between.

Figure 7 Processor Block Read

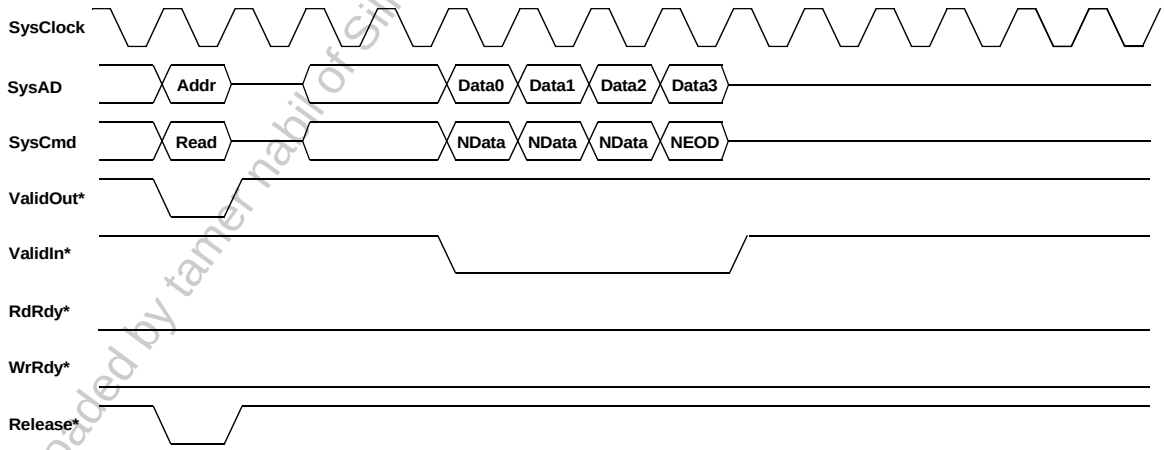
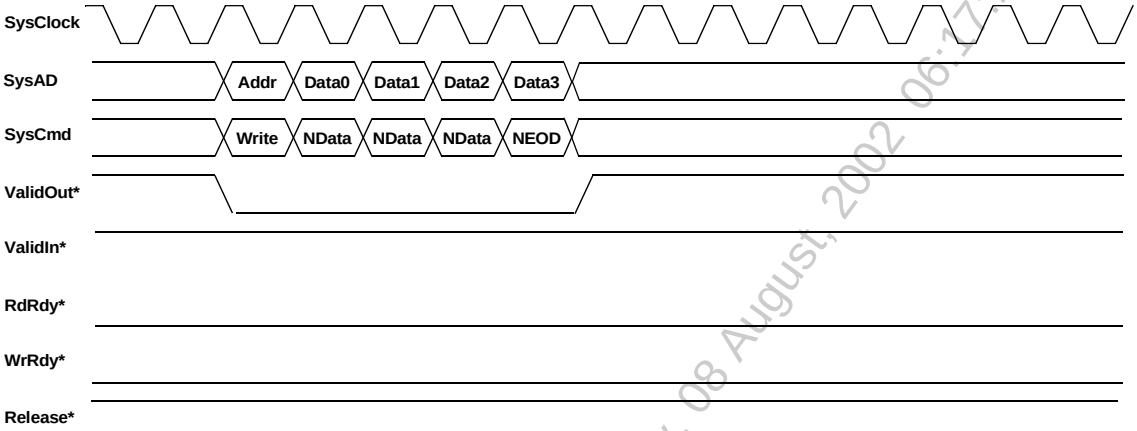


Figure 8 shows a processor block write using write response pattern DDDD, or code 0, of the boot-time mode select options.

Figure 8 Processor Block Write



3.26 Enhanced Write Modes

The RM5261A implements two enhancements to the original R4000 write mechanism: Write Reissue and Pipeline Writes. The original R4000 allowed a write address cycle on the **SysAD** bus only once every four SysClock cycles. Hence for a non-block write, this meant that two out of every four cycles were wait states.

Pipelined write mode eliminates these two wait states by allowing the processor to drive a new write address onto the bus immediately after the previous write data cycle. This allows for higher **SysAD** bus utilization. However, at high bus frequencies the processor may drive a subsequent write onto the bus prior to the time the external agent deasserts **WrRdy***, indicating that it can not accept another write cycle. This can cause the write cycle to be missed.

Write reissue mode is an enhancement to pipelined write mode and allows the processor to reissue missed write cycles. If **WrRdy*** is deasserted during the issue phase of a write operation, the cycle is aborted by the processor and reissued at a later time.

In write reissue mode, a write rate of one write every two bus cycles can be achieved. Pipelined writes have the same two bus cycle write repeat rate, but can issue one additional write following the deassertion of **WrRdy***.

3.27 External Requests

The External Request pin, **ExtRqst***, is asserted by the external agent when it requires mastership of the system interface, either to perform an independent transfer or to write to the interrupt register within the RM5261A. An independent transfer is a data transfer between two external agents or between an external agent and memory or peripheral on the system interface. Following the asserting of the **ExtRqst***, the RM5261A tri-states its drivers allowing the external agent to use the system interface buses to complete an independent transfer. The external agent is responsible for returning mastership of the system interface to the RM5261A when it has completed the independent transfer and does so by executing an External Null cycle.

3.28 Interrupt Handling

The RM5261A supports a dedicated interrupt vector. When enabled by the real time executive (by setting a bit in the Cause register), interrupts vector to a specific address that is not shared with any of the other exception types. This capability eliminates the need to go through the normal software routine for exception decode and dispatch, thereby lowering interrupt latency.

3.29 Standby Mode

The RM5261A provides a means to reduce the amount of power consumed by the internal core when the CPU is not performing any useful operations. This state is known as Standby Mode.

Executing the WAIT instruction enables interrupts and causes the processor to enter Standby Mode. If the **SysAD** bus is idle when the wait instruction completes the W pipe stage, the internal processor clock stops and the pipeline is suspended. The phase lock loop, or PLL, internal timer/ counter, and the "wake up" input pins: **Int[5:0]***, **NMI***, **ExtReq***, **Reset***, and **ColdReset*** continue to operate in their normal fashion. If the **SysAD** bus is not idle when the WAIT instruction completes the W pipe-stage, then the WAIT is treated as a NOP until the bus operation is completed. Once the processor is in Standby, any interrupt, including the internally generated timer interrupt, causes the processor to exit Standby mode and resume operation where it left off. The WAIT instruction is typically inserted in the idle loop of the operating system or real time executive.

3.30 JTAG Interface

The RM5261A interface supports JTAG Test Access Port (TAP) boundary scan in conformance with the IEEE 1149.1 specification. The JTAG interface is especially helpful for checking the integrity of the processors pin connections.

3.31 Boot-Time Options

Fundamental operational modes for the processor are initialized by the boot-time mode control interface. This serial interface operates at a very low frequency (SysClock divided by 256). The low frequency operation allows the initialization information to be kept in a low cost EPROM or system interface ASIC.

Immediately after the $\mathbf{V_{CC}OK}$ signal is asserted, the processor reads a serial bit stream of 256 bits to initialize all the fundamental operational modes. ModeClock runs continuously from the assertion of $\mathbf{V_{CC}OK}$.

3.32 Boot-Time Modes

The boot-time serial mode stream is defined in Table 4. Bit 0 is the bit presented to the processor as the first bit in the stream when $\mathbf{V_{CC}OK}$ is asserted. Bit 255 is the last bit transferred.

Table 4 Boot-Time Mode Bit Stream

Mode bit	Description	Mode bit	Description
0	reserved (must be zero)	15	Reserved: Must be zero
4:1	Write-back data rate 0: DDDD 1: DDxDDx 2: DDxxDDxx 3: DxDxDxDx 4: DDxxxDDxxx 5: DDxxxxDDxxxx 6: DxxDxxDxxDxx 7: DDxxxxxxDDxxxxxx 8: DxxxDxxxDxxxDxxx 9-15 reserved	17:16	System configuration identifiers - software visible in Config[21..20] register
7:5	Pclock to SysClock Multiplier Mode Bits 7:5 / Mode Bit 20=0 / Mode Bit 20=1 000 Multiply by 2 n/a 001 Multiply by 3 n/a 010 Multiply by 4 n/a 011 Multiply by 5 Multiply by 2.5 100 Multiply by 6 n/a 101 Multiply by 7 Multiply by 3.5 110 Multiply by 8 n/a 111 Multiply by 9 Multiply by 4.5	19:18	Reserved: Must be zero
8	Specifies byte ordering. Logically ORed with BigEndian input signal. 0: Little endian 1: Big endian	20	Select Pclock to SysClock Multiply Mode 0: Integer Multipliers 1: Half-Integer Multipliers
10:9	Non-Block Write Protocol 00: R4000 compatible 01: reserved 10: pipelined 11: write re-issue	21	External Bus Width 0: 64-bit 1: 32-bit
11	Timer Interrupt Enable/Disable 0: Enable the timer interrupt on **Int5*** 1: Disable the timer interrupt on **Int5***	22	VccIO Setting 0: VccIO = 3.3V 1: VccIO = 2.5V
12	Reserved: Must be zero	255:23	Reserved: Must be zero
14:13	Output driver strength - 100% = fastest 00: 67% strength 01: 50% strength 10: 100% strength 11: 83% strength		

4 Pin Descriptions

The following is a list of interface, interrupt, and miscellaneous pins available on the RM5261A. An asterisk (*) at the end of the the signal name denotes active-low.

Table 5 System Interface

Pin Name	Type	Description
ExtRqst*	Input	External Request Signals that the system interface is submitting an external request.
Release*	Output	Release Interface Signals that the processor is releasing the system interface to slave state.
RdRdy*	Input	Read Ready Signals that an external agent can now accept a processor read.
WrRdy*	Input	Write Ready Signals that an external agent can now accept a processor write request.
ValidIn*	Input	Valid Input Signals that an external agent is now driving a valid address or data on the **SysAD** bus and a valid command or data identifier on the **SysCmd** bus.
ValidOut*	Output	Valid Output Signals that the processor is now driving a valid address or data on the **SysAD** bus and a valid command or data identifier on the **SysCmd** bus.
SysAD[63:0]	Input/Output	System Address/Data bus A 64-bit address and data bus for communication between the processor and an external agent.
SysADC[7:0]	Input/Output	System Address/Data check bus An 8-bit bus containing parity check bits for the **SysAD** bus during data cycles.
SysCmd[8:0]	Input/Output	System Command/Data identifier bus A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	Input/Output	Reserved for system Command/Data identifier bus parity For the RM5261A, unused on input and zero on output.

Table 6 Clock/Control Interface

Pin Name	Type	Description
SysClock	Input	System Clock Master clock input used as the system interface reference clock. All output timings are relative to this input clock. Pipeline operation frequency is derived by multiplying this clock up by the factor selected during boot initialization.
VccP	Input	Quiet **Vcc** for PLL Quiet **Vcc** for the internal phase locked loop. Must be connected to **VccInt** through a filter circuit.
V_{SS}P	Input	Quiet **V_{SS}** for PLL Quiet **V_{SS}** for the internal phase locked loop. Must be connected to **V_{SS}** through a filter circuit.

Table 7 Interrupt Interface

Pin Name	Type	Description
Int[5:0]*	Input	Interrupt Six general processor interrupts, bit-wise ORed with bits 5:0 of the interrupt register.
NMI*	Input	Non-maskable interrupt Non-maskable interrupt, ORed with bit 6 of the interrupt register.

Table 8 JTAG Interface

Pin Name	Type	Description
JTDI	Input	JTAG data in JTAG serial data in.
JTCK	Input	JTAG clock input JTAG serial clock input.
JTDO	Output	JTAG data out JTAG serial data out.
JTMS	Input	JTAG command JTAG command signal, signals that the incoming serial data is command data.

Table 9 Initialization Interface

Pin Name	Type	Description
BigEndian	Input	Allows the system to change the processor addressing mode without rewriting the mode ROM.
V_{CC}OK	Input	**V_{CC}** is OK When asserted, this signal indicates to the RM5261A that both power supplies has been above the recommended value for more than 100 milliseconds and will remain stable. The assertion of **V_{CC}OK** initiates the reading of the boot-time mode control serial stream.
ColdReset*	Input	Cold reset This signal must be asserted for a power on reset or a cold reset. ColdReset must be de-asserted synchronously with **SysClock**.
Reset*	Input	Reset This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. **Reset** must be de-asserted synchronously with **SysClock**.
ModeClock	Output	Boot mode clock Serial boot-mode data clock output at the system clock frequency divided by 256.
ModeIn	Input	Boot mode data in Serial boot-mode data input.

Table 10 Power Supply

Pin Name	Type	Description
V_{CC}Int	Input	Power supply for core.
V_{CC}IO	Input	Power supply for I/O.
V_{SS}	Input	Ground return.

5 Absolute Maximum Ratings[1]

Symbol	Rating	Limits	Unit
V_{TERM}	Terminal Voltage with respect to V_{SS}	–0.5[2] to +3.9	V
T_{CASE}	Operating Temperature		
	Commercial	0 to +85	°C
	Industrial	–45 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{IN}	DC Input Current	±20[3]	mA
I_{OUT}	DC Output Current	±20[4]	mA

Notes:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = -2.0 V for pulse width less than 15 ns. V_{IN} should not exceed 3.9 Volts.
3. When V_{IN} < 0V or V_{IN} > $V_{CC}IO$
4. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

6 Recommended Operating Conditions

Grade	CPU Speed	Case Temperature	V_{SS}	$V_{CC}Int$	$V_{CC}IO$	$V_{CC}P$	$V_{SS}P$
Commercial	250 – 350 MHz	0°C to +85°C	0 V	1.57 V to 1.85 V	3.15 V to 3.45 V or 2.3 V to 2.7 V	1.57 V to 1.85 V	0 V
	400 MHz	0°C to +70°C	0 V	1.8 V ± 50 mV	3.15 V to 3.45 V	1.8 V ± 50 mV	0 V
Industrial	300 MHz	-40°C to +85°C	0 V	1.57 V to 1.85 V	3.15 V to 3.45 V or 2.3 V to 2.7 V	1.57 V to 1.85 V	0 V

Notes:

1. **$V_{CC}IO$** should not exceed **$V_{CC}Int$** by greater than 2.0 V during the power-up sequence.
2. Applying a logic high state to any I/O pin before **$V_{CC}Int$** becomes stable is not recommended.
3. As specified in IEEE 1149.1 (JTAG), the **JTMS** pin must be held high during reset to avoid entering JTAG test mode.
4. **$V_{CC}P$** must be connected to **$V_{CC}Int$** through a passive filter circuit. **$V_{SS}P$** must be connected to **V_{SS}** through a passive filter circuit. See the RM5200 User's Manual for the recommended filter circuit.

7 DC Electrical Characteristics

$V_{CC}IO$ = 3.15 V – 3.45 V

Parameter	Minimum	Maximum	Conditions
V_{OL}		0.2 V	$\|I_{OUT}\|$= 100 µA
V_{OH}	VccIO - 0.2 V		
V_{OL}		0.4 V	$\|I_{OUT}\|$ = 2 mA
V_{OH}	2.4 V		
V_{IL}	-0.3 V	0.8 V	
V_{IH}	2.0 V	VccIO + 0.3 V	
I_{IN}		±15 µA ±15 µA	V_{IN} = 0 V_{IN} = VccIO

$V_{CC}IO$ = 2.3 V – 2.7 V

Parameter	Minimum	Maximum	Conditions
V_{OL}		0.2 V	$\|I_{OUT}\|$= 100 µA
V_{OH}	2.1 V		
V_{OL}		0.4 V	$\|I_{OUT}\|$ = 1 mA
V_{OH}	2.0		
V_{OL}		0.7 V	$\|I_{OUT}\|$ = 2 mA
V_{OH}	1.7		
V_{IL}	–0.3 V	0.7 V	
V_{IH}	1.7 V	VccIO + 0.3 V	
I_{IN}		±15 µA ±15 µA	V_{IN} = 0 V_{IN} = VccIO

8 Power Consumption

Parameter		Conditions	CPU Speed			
			250 MHz	300 MHz	350 MHz	400 MHz
			Max[1]	Max[1]	Max[1]	Max[1]
V_{CC}Int Power (mWatts)[3]	standby		350	350	350	600
	active	Maximum with no FPU operation[2]	1150	1350	1450	1800
		Maximum worst case instruction mix	1250	1400	1600	2100

Notes:

1. Maximum supply voltage (V_{CC}Int) with maximum temperature (TCase).
2. Dhrystone 2.1 instruction mix.
3. V_{CC}IO supply power is application dependant, but typically <20% of V_{CC}Int.

9 AC Electrical Characteristics

9.1 Capacitive Load Deration

Parameter	Symbol	Min	Max	Units
Load Derate	C_{LD}	—	2	ns/25pF

9.2 Clock Parameters

Parameter	Symbol	Test Conditions	CPU Speed								Units
			250 MHz		300 MHz		350 MHz		400 MHz		
			Min	Max	Min	Max	Min	Max	Min	Max	
SysClock High	t_{SCH}	Transition ≤ 2ns	3		3		3		3		ns
SysClock Low	t_{SCL}	Transition ≤ 2ns	3		3		3		3		ns
SysClock Frequency[1]			33	125	33	125	33	125	33	133	MHz
SysClock Period	t_{SCP}		8	30	8	30	8	30	7.5	30	ns
Clock Jitter for SysClock	t_{JI}			±150		±150		±150		±150	ps
SysClock Rise Time	t_{CR}			2		2		2		2	ns
SysClock Fall Time	t_{CF}			2		2		2		2	ns
ModeClock Period	$t_{ModeCKP}$			256		256		256		256	t_{SCP}
JTAG Clock Period	$t_{JTAGCKP}$		4		4		4		4		t_{SCP}

Notes:

1. Operation of the RM5261A is only guaranteed with the Phase Lock Loop Enabled.

9.3 System Interface Parameters[1]

Parameter[1]	Symbol	Conditions	CPU Speed				Units
			250 to 350 MHz		400 MHz		
			Min	Max	Min	Max	
Data Output[2,3]	t_{DO}	mode14..13 = 10[5,6] (fastest)	1.0	5.0	1.0	4.75	ns
		mode14..13 = 01[5,6] (slowest)	1.0	6.0	1.0	5.75	ns
Data Setup[4]	t_{DS}[6]	t_{rise} = see above table	2.5		2.0		ns
Data Hold[4]	t_{DH}	t_{fall} = see above table	1.0		1.0		ns

Notes:

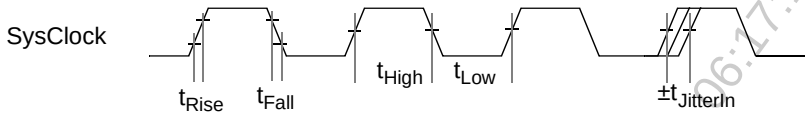
1. Timings are measured from 0.425 x **V_{CC}IO** of clock to 0.425 x **V_{CC}IO** of signal for 3.3V I/O. Timings are measured from 0.48 x **V_{CC}IO** of clock to 0.48 *x* **V_{CC}IO** of signal for 2.5V I/O.
2. Capacitive load for all maximum output timings is 50 pF. Minimum output timings are for theoretical no load condition-untested.
3. Data Output timing applies to all signal pins whether tristate I/O or output only.
4. Setup and Hold parameters apply to all signal pins whether tristate I/O or input only.
5. Only mode 14:13 = 10 is tested and guaranteed.
6. Data shown is for 3.3 V I/O. For 2.5 V I/O (250 to 350 MHz CPU speeds only) derate all times by .5 nS.

9.4 Boot-Time Interface Parameters

Parameter	Symbol	Min	Max	Units
Mode Data Setup	t_{DS}	4		SysClock cycles
Mode Data Hold	t_{DH}	0		SysClock cycles

10 Timing Diagrams

Figure 9 Clock Timing



10.1 System Interface Timing (SysAD, SysCmd, ValidIn*, ValidOut*, etc.)

Figure 10 Input Timing

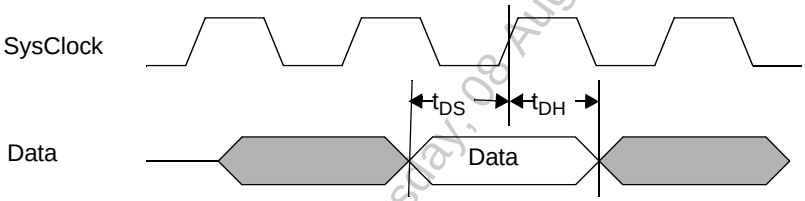
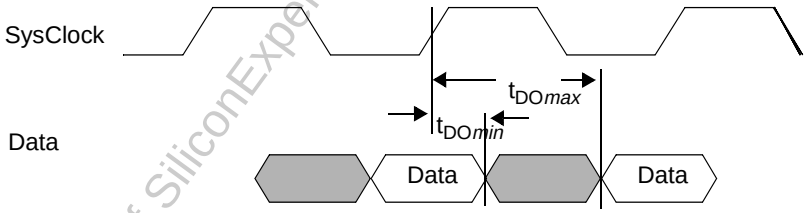
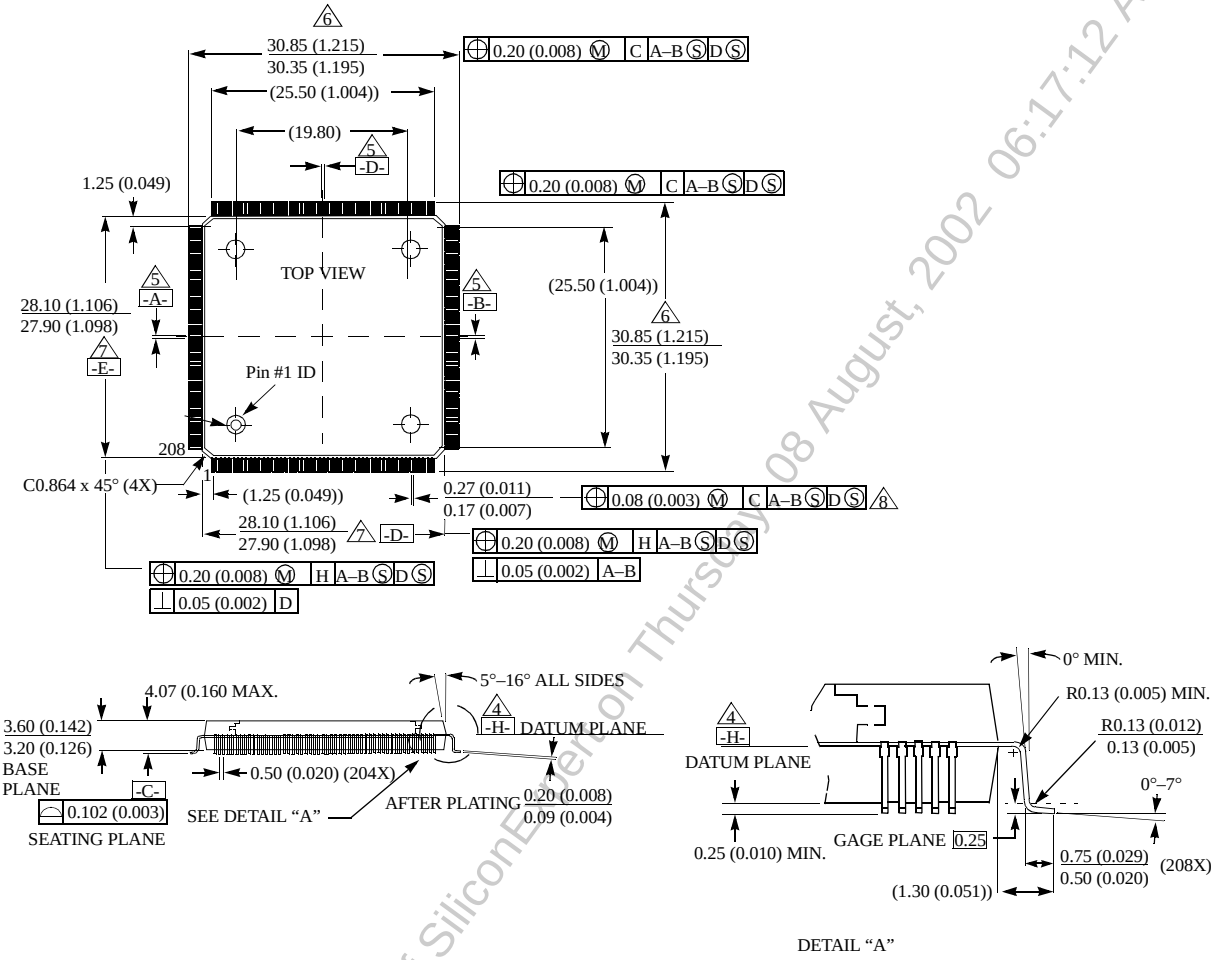


Figure 11 Output Timing



11 Packaging Information



DETAIL "A"

Notes

1. Package dimensions conform to JEDEC MS–029(FA–1).
2. Controlling dimensions: millimeters. Dimensions in inches are shown in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5 – 1982.
4. Datum plane "H" is located at the mold parting line and is coincident with the lead exits the plastic body at bottom of the parting line.
5. Datums "A–B" and "D" to be determined at datum plane "H".
6. To be determined at the seating plane "C".
7. These dimensions to be determined at datum plane "H". Dimensions "D" and "E" do not include mold protrusion. Allowable protrusion is 0.25/0.10" per side.
8. Lead width does not include damber protrusion. Allowable damber protrusion shall be 0.08 mm/0.003" total in excess of this dimension at the maximum material condition. Dambar cannot be located on the lower radius of the foot.
9. Pin numbers start with pin 1 and continue counter-clockwise to pin 208 when viewed from the top.

12 RM5261A 208-QFP Package Numerical Pinout

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	$V_{CC}IO$	43	SysAD47	85	SysCmd8	127	V_{SS}	169	SysAD30
2	NC	44	$V_{CC}IO$	86	SysCmdP	128	SysAD20	170	SysAD62
3	NC	45	V_{SS}	87	$V_{CC}Int$	129	SysAD52	171	$V_{CC}IO$
4	$V_{CC}IO$	46	ModeClock	88	Vss	130	SysAD21	172	V_{SS}
5	V_{SS}	47	JTDO	89	$V_{CC}Int$	131	SysAD53	173	SysAD31
6	SysAD4	48	JTDI	90	V_{SS}	132	$V_{CC}IO$	174	SysAD63
7	SysAD36	49	JTCK	91	$V_{CC}IO$	133	V_{SS}	175	SysADC2
8	SysAD5	50	JTMS	92	V_{SS}	134	SysAD22	176	SysADC6
9	SysAD37	51	$V_{CC}IO$	93	Int0*	135	SysAD54	177	$V_{CC}Int$
10	$V_{CC}Int$	52	V_{SS}	94	Int1*	136	$V_{CC}Int$	178	V_{SS}
11	V_{SS}	53	NC	95	Int2*	137	V_{SS}	179	SysADC3
12	SysAD6	54	NC	96	Int3*	138	SysAD23	180	SysADC7
13	SysAD38	55	NC	97	Int4*	139	SysAD55	181	$V_{CC}IO$
14	$V_{CC}IO$	56	$V_{CC}IO$	98	Int5*	140	SysAD24	182	V_{SS}
15	V_{SS}	57	V_{SS}	99	$V_{CC}IO$	141	SysAD56	183	SysADC0
16	SysAD7	58	ModeIn	100	V_{SS}	142	$V_{CC}IO$	184	SysADC4
17	SysAD39	59	RdRdy*	101	NC	143	V_{SS}	185	$V_{CC}Int$
18	SysAD8	60	WrRdy*	102	NC	144	SysAD25	186	V_{SS}
19	SysAD40	61	ValidIn*	103	NC	145	SysAD57	187	SysADC1
20	$V_{CC}Int$	62	ValidOut*	104	NC	146	$V_{CC}Int$	188	SysADC5
21	V_{SS}	63	Release*	105	$V_{CC}IO$	147	V_{SS}	189	SysAD0
22	SysAD9	64	$V_{CC}P$	106	NMI*	148	SysAD26	190	SysAD32
23	SysAD41	65	$V_{SS}P$	107	ExtRqst*	149	SysAD58	191	$V_{CC}IO$
24	$V_{CC}IO$	66	SysClock	108	Reset*	150	SysAD27	192	V_{SS}
25	V_{SS}	67	$V_{CC}Int$	109	ColdReset*	151	SysAD59	193	SysAD1
26	SysAD10	68	V_{SS}	110	$V_{CC}OK$	152	$V_{CC}IO$	194	SysAD33
27	SysAD42	69	$V_{CC}IO$	111	BigEndian	153	V_{SS}	195	$V_{CC}Int$

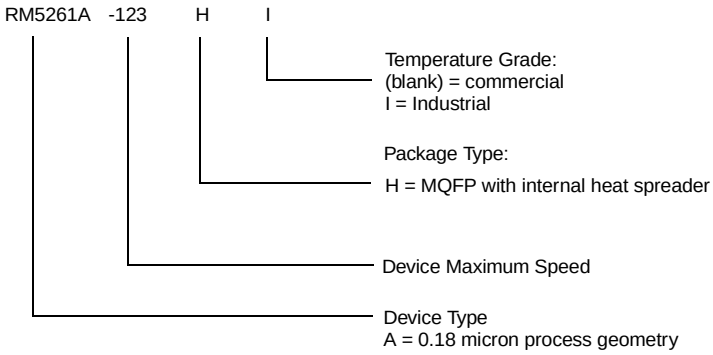
Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
28	SysAD11	70	V_{SS}	112	$V_{CC}IO$	154	NC	196	V_{SS}
29	SysAD43	71	$V_{CC}Int$	113	V_{SS}	155	NC	197	SysAD2
30	$V_{CC}Int$	72	V_{SS}	114	SysAD16	156	V_{SS}	198	SysAD34
31	V_{SS}	73	SysCmd0	115	SysAD48	157	NC	199	SysAD3
32	SysAD12	74	SysCmd1	116	$V_{CC}Int$	158	NC	200	SysAD35
33	SysAD44	75	SysCmd2	117	V_{SS}	159	NC	201	$V_{CC}IO$
34	$V_{CC}IO$	76	SysCmd3	118	SysAD17	160	NC	202	V_{SS}
35	V_{SS}	77	$V_{CC}IO$	119	SysAD49	161	$V_{CC}IO$	203	NC
36	SysAD13	78	V_{SS}	120	SysAD18	162	V_{SS}	204	NC
37	SysAD45	79	SysCmd4	121	SysAD50	163	SysAD28	205	NC
38	SysAD14	80	SysCmd5	122	$V_{CC}IO$	164	SysAD60	206	NC
39	SysAD46	81	$V_{CC}IO$	123	V_{ss}	165	SysAD29	207	$V_{CC}IO$
40	$V_{CC}Int$	82	V_{SS}	124	SysAD19	166	SysAD61	208	V_{SS}
41	V_{SS}	83	SysCmd6	125	SysAD51	167	$V_{CC}Int$		
42	SysAD15	84	SysCmd7	126	$V_{CC}Int$	168	V_{SS}		

13 RM5261A 208-QFP Package Alphabetical Pinout

Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin
BigEndian	111	SysAD4	6	SysAD46	39	V_{CC}Int	40	V_{SS}	15
ColdReset*	109	SysAD5	8	SysAD47	43	V_{CC}Int	67	V_{SS}	21
ExtRqst*	107	SysAD6	12	SysAD48	115	V_{CC}Int	71	V_{SS}	25
Int0*	93	SysAD7	16	SysAD49	119	V_{CC}Int	87	V_{SS}	31
Int1*	94	SysAD8	18	SysAD50	121	V_{CC}Int	89	V_{SS}	35
Int2*	95	SysAD9	22	SysAD51	125	V_{CC}Int	116	V_{SS}	41
Int3*	96	SysAD10	26	SysAD52	129	V_{CC}Int	126	V_{SS}	45
Int4*	97	SysAD11	28	SysAD53	131	V_{CC}Int	136	V_{SS}	52
Int5*	98	SysAD12	32	SysAD54	135	V_{CC}Int	146	V_{SS}	57
JTCK	49	SysAD13	36	SysAD55	139	V_{CC}Int	167	V_{SS}	68
JTDI	48	SysAD14	38	SysAD56	141	V_{CC}Int	177	V_{SS}	70
JTDO	47	SysAD15	42	SysAD57	145	V_{CC}Int	185	V_{SS}	72
JTMS	50	SysAD16	114	SysAD58	149	V_{CC}Int	195	V_{SS}	78
ModeClock	46	SysAD17	118	SysAD59	151	V_{CC}IO	1	V_{SS}	82
ModeIn	58	SysAD18	120	SysAD60	164	V_{CC}IO	4	V_{SS}	88
NC	2	SysAD19	124	SysAD61	166	V_{CC}IO	14	V_{SS}	90
NC	3	SysAD20	128	SysAD62	170	V_{CC}IO	24	V_{SS}	92
NC	53	SysAD21	130	SysAD63	174	V_{CC}IO	34	V_{SS}	100
NC	54	SysAD22	134	SysADC0	183	V_{CC}IO	44	V_{SS}	113
NC	55	SysAD23	138	SysADC1	187	V_{CC}IO	51	V_{SS}	117
NC	101	SysAD24	140	SysADC2	175	V_{CC}IO	56	V_{SS}	123
NC	102	SysAD25	144	SysADC3	179	V_{CC}IO	69	V_{SS}	127
NC	103	SysAD26	148	SysADC4	184	V_{CC}IO	77	V_{SS}	133
NC	104	SysAD27	150	SysADC5	188	V_{CC}IO	81	V_{SS}	137
NC	154	SysAD28	163	SysADC6	176	V_{CC}IO	91	V_{SS}	143
NC	155	SysAD29	165	SysADC7	180	V_{CC}IO	99	V_{SS}	147
NC	157	SysAD30	169	SysClock	66	V_{CC}IO	105	V_{SS}	153

Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin
NC	158	SysAD31	173	SysCmd0	73	$V_{CC}IO$	112	Vss	156
NC	159	SysAD32	190	SysCmd1	74	$V_{CC}IO$	122	V_{SS}	162
NC	160	SysAD33	194	SysCmd2	75	$V_{CC}IO$	132	V_{SS}	168
NC	203	SysAD34	198	SysCmd3	76	$V_{CC}IO$	142	V_{SS}	172
NC	204	SysAD35	200	SysCmd4	79	$V_{CC}IO$	152	V_{SS}	178
NC	205	SysAD36	7	SysCmd5	80	$V_{CC}IO$	161	V_{SS}	182
NC	206	SysAD37	9	SysCmd6	83	$V_{CC}IO$	171	V_{SS}	186
NMI*	106	SysAD38	13	SysCmd7	84	$V_{CC}IO$	181	V_{SS}	192
RdRdy*	59	SysAD39	17	SysCmd8	85	$V_{CC}IO$	191	V_{SS}	196
Release*	63	SysAD40	19	SysCmdP	86	$V_{CC}IO$	201	V_{SS}	202
Reset*	108	SysAD41	23	ValidIn*	61	$V_{CC}IO$	207	V_{SS}	208
SysAD0	189	SysAD42	27	ValidOut*	62	$V_{CC}OK$	110	$V_{SS}P$	65
SysAD1	193	SysAD43	29	$V_{CC}Int$	10	$V_{CC}P$	64	WrRdy*	60
SysAD2	197	SysAD44	33	$V_{CC}Int$	20	V_{SS}	5		
SysAD3	199	SysAD45	37	$V_{CC}Int$	30	V_{SS}	11		

14 Ordering Information



Valid Combinations

RM5261A–250–H

RM5261A–300–H

RM5261A–300–HI (contact sales prior to design)

RM5261A–350–H

RM5261A–400–H